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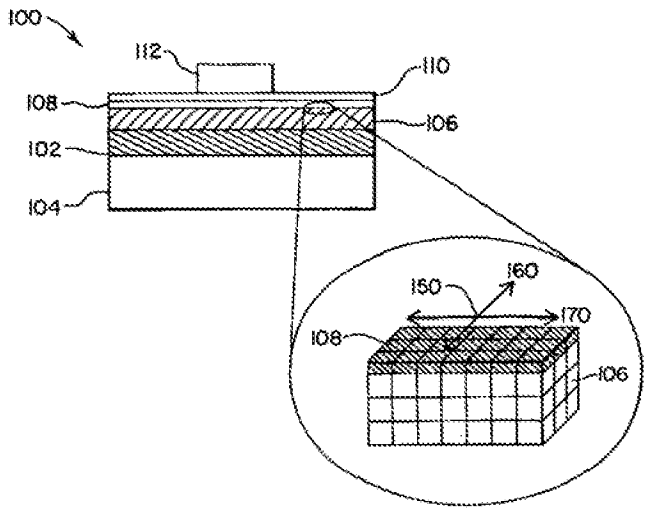

(57) Abstract: A CMOS inverter having a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer; and a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of the nMOSFET are formed in the strained surface layer. Another embodiment provides an integrated circuit having a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on the Si substrate, and a strained layer on the relaxed $Si_{1-x}Ge_x$ layer; and a p transistor and an n transistor formed in the heterostructure, wherein the strained layer comprises the channel of the n transistor and the p transistor, and the n transistor and the p transistor are interconnected in a CMOS circuit.

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CMOS INVERTER CIRCUITS UTILIZING STRAINED SILICON SURFACE CHANNEL MOSFETS

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/250,985 filed December 4, 2000.

This application is a continuation-in-part of patent applications Ser. No. 09/884,172 and Ser. No. 09/884,517, both filed June 19, 2001.

BACKGROUND OF THE INVENTION

The invention relates to the field of *strained silicon* (silicon where the crystallographic structure has been modified to increase carrier mobility) surface channel MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), and, in particular, to using these MOSFETs in CMOS (Complimentary Metal Oxide Semiconductor which contain both a NMOS and PMOS device) inverters (a circuit where the output waveform rises and falls with the opposite waveform at the input) as well as in other integrated circuits. Inverter circuits are used as basic building blocks of all Very Large Scale Integrated (VLSI) designs since they allow for a basic switch (on or off state device). Hence, a basic inverter circuit of VLSI design can be used ubiquitously. The design of these CMOS inverters are so essential to VLSI design that detail trade-offs are made between the types of substrates used, the size of the devices used in the basic CMOS inverter circuit, as well as the semiconductor processing equipment and semiconductor materials used to make these devices.

From the 1970's to the year 2001, gate lengths (the physical distance between the source and the drain of a MOSFET device) have decreased by two orders of magnitude in order to speed up MOSFET devices. This decrease of gate lengths has resulting in a 30% improvement in the price/performance per year as well as drastically improved density (number of MOSFET devices per unit area) and has drastically reduced the power needs of the devices.

One way to increase the speed, improve density and lower power of the MOSFET devices is to shrink the MOSFET devices to smaller physical dimensions by moving the devices source and drain regions closer together (smaller MOSFET gate length). This has been the main direction of the semiconductor industry and this has been successfully implemented by enhancing and improving the semiconductor process technology, e.g. optical photolithography tools, defect cleaning tools, etc., and enhancing and improving the

semiconductor materials e.g. photoresist materials, metallurgical materials, etc.

As MOSFET device sizes are made smaller and are designed in the sub-micron regime, the associated cost of new semiconductor tools and semiconductor materials can be prohibitive. For instance, a new state of the art CMOS facility utilizing these new semiconductor tools and semiconductor materials for use in semiconductor fabrication can cost more than $2 billion dollars per semiconductor fabrication plant. This is a large investment of money considering that the semiconductor processing equipment and the semiconductor materials are generally only useful for two scaling generations (3-4 years).

In addition to economic constraints, physically shrinking device size is quickly approaching solid state physics constraints of the device materials. Fundamental solid state physics limitations such as gate oxide leakage and source/drain resistance make continued mininmization beyond 0.1 micrometers (μm) gate length difficult if not impossible to maintain.

In order to cope with both the costs of advanced semiconductor processing tooling and equipment and the costs of the semiconductor materials and the limitations of the solid state physics limitations, semiconductor researchers are actively seeking new substrate materials that are enhancements over bulk silicon. These new substrate materials may allow the MOSFET device to obtain increases in speed and reductions in power without necessarily shrinking device size. These enhancements may lessen or put off new semiconductor processing tooling and new semiconductor materials for a generation..

One new substrate material used in the art to enhance speed and reduce power is the use of Gallium Arsenide (GaAs), which has higher electron mobility than the bulk silicon substrate materials. However, there is a limitation in the use in Complimentary FET devices (required for circuit design) where there are both N doped FET's (NFET's) where electron flow is predominant and P doped FET's (PFET's) where hole flow is predominant. The NFET devices will have higher speed because of the higher electron mobility in GaAs, but the PFET devices do not see the larger increase in their speed since the hole mobility is not dramatically enhanced. This limitation causes an asymmetry problem for complementary FET architecture uses in circuits, like inverters.

In addition to this limitation, there is a further limitation since the GaAs devices are usually fabricated with Schottky gates, which have larger leakage currents. These leakage currents are orders of magnitudes higher than MOS structures. The excess leakage causes a limitation since it leads to an increase in the "off-state" power consumption of circuits,

which makes it unacceptable for highly functional circuits. Schottky gates have a further limitation in that the processing does not allow for self-aligned gate technology, which is enjoyed by MOS structures, and thus typically FETs on GaAs have larger gate-to-source and gate-to-drain resistances. Finally, an additional limitation is that GaAs processing does not enjoy the same economies of scale that have caused silicon technologies to thrive, since they are not widely used in high volume semiconductor processing. As a result, wide-scale production of GaAs circuits would be extremely costly to implement.

Another new substrate material used in the art to enhance speed and reduce power is the use of fabricating devices on silicon-on-insulator (SOI) substrates. In a SOI substrate based device, a buried oxide layer prevents the device channel from being fully depleting. Partially depleted devices offer improvements in the junction area capacitance, the device body effect, and the gate-to-body coupling capacitances, all which lead to faster devices and lower power devices. In the best-case scenario, these device improvements will result in up to 18% enhancement in circuit speed. However, there is a limitation since this improved performance comes at a cost. The partially depleted floating body of the FET device causes an uncontrolled lowering of the threshold voltage, known as the floating body effect. This phenomenon increases the off-state leakage of the transistor and thus offsets some of the potential performance advantages. Circuit designers can extract enhancements through design changes at the architectural level. However, this level of redesign can be costly and thus is not economically advantageous for all Si CMOS products.

In addition to this limitation, there is a further limitation that the reduced junction capacitance of SOI devices is less important for high functionality circuits where the interconnect capacitance is dominant. As a result, the enhancement offered by SOI devices is limited in its scope.

Another new substrate material used in the art to enhance speed and reduce power is the use of mobility enhancement in devices created on a *strained silicon* substrate. To date, efforts have focused on circuits that employ a *buried channel device* for the P doped MOSFET (PMOS), and a *surface channel* device for the N doped MOSFET (NMOS). This arrangement provides the maximum mobility enhancement; however, there are limitations. At high fields, the *buried channel PMOS* device performance is complex due to the activation of two carrier channels, and therefore device circuit design, as well as the semiconductor process that makes these buried channel PMOS devices, becomes difficult.

In addition to this limitation, there is a further limitation that in order to create a buried channel PMOS device and surface channel NMOS device on the same *strained*

silicon substrate, the cost of semiconductor fabrication required is significantly higher compared to that for bulk silicon processing.

It is first object of this invention to create a high speed, low power high density CMOS inverter comprising a surface channel PMOS and surface channel NMOS in a *strained silicon* substrate, where both PMOS and NMOS devices are on the same monolithic substrate to keep cost and complexity down.

It is another object of this invention to create strained silicon surface channel substrates that can be incorporated with SOI technology in order to provide ultra-high speed/low power circuits.

It is another object of this invention to create a strained silicon surface channel CMOS inverter circuit built on a bonded SiGe structure.

It is another object of this invention to create strained silicon surface channel devices that can be fabricated with standard silicon CMOS processing tools and semiconductor materials allowing for performance enhancement with no additional capital expenditures.

It is another object of this invention to create high speed or high frequency of operation CMOS inverter circuits using PMOS or NMOS strained silicon surface channel devices while keeping the power constant. This scenario is useful for applications such as desktop computers where the speed is more crucial than the power consumption.

It is another object of this invention to create a high speed or high frequency of operation CMOS inverter circuit on a strained silicon surface channel device while keeping the power constant. By judiciously swapping a strained silicon substrate for the bulk silicon substrate in the process, and taking into account the changes in process (implants etc.), certain circuit and design changes are made (supporting CMOS) to account for the increase in speeds for the CMOS inverter so that race conditions do not occur. This scenario is useful for applications such as desktop computers where the speed is more crucial than the power consumption.

It is another object of this invention to create even higher speed or higher frequency of operation CMOS inverter circuit while keeping the power constant by employing strained silicon improvements with constant V_{DD}. This scenario is useful for applications such as desktop computers where the speed is more crucial than the power consumption.

It is another object of this invention to create a reduced power CMOS inverter circuit used at constant speed or frequency of operation. This situation is most useful for portable applications that operate off of a limited power supply.

It is another object of this invention to create more dense inverters based upon

PMOS or NMOS strained silicon surface channel devices.

It is another object of this invention to create a balanced operation CMOS inverter circuit.

It is another object of this invention to create a balanced operation CMOS inverter circuit with device capacitance being dominant over wiring capacitance.

It is another object of this invention to create a balanced operation CMOS inverter circuit with device capacitance being dominant over device capacitance.

It is another object of this invention to create a strained silicon surface channel CMOS inverter circuit for both long and short channel devices.

It is another object of this invention to create strained silicon surface channel devices that are scalable (shrinkable in dimensions) using the standard silicon substrate scaling tools (photolithography etc.) and materials. Thus scaling can be implemented in both long and short channel strained silicon surface devices.

It is another object of this invention to create strained silicon surface channel technology, which is similar to bulk silicon technology so that strained silicon channel devices can achieve all the other enhancement methods of bulk silicon technology, e.g. isolation, implantation, wiring, etc.

It is another object of this invention to use strained silicon surface channel CMOS circuits to build many basic digital circuits building blocks.

SUMMARY OF THE INVENTION

In accordance with the invention, the performance of a silicon CMOS inverter is enhanced by increasing the electron and hole mobility. This enhancement is achieved through deploying surface channel, strained-silicon, which is epitaxially grown on an engineered SiGe/Si substrate. Both the n-type and p-type channels (NMOS and PMOS) are surface channel, *enhancement* mode devices. This technique allows the CMOS inverter performance to be improved (density, power, speed, or a combination thereof) without adding complexity to circuit fabrication or design.

The Strained Silicon Substrate

When silicon is placed under tension, the degeneracy of the conduction band splits, forcing two valleys to be occupied instead of six. As a result, the in-plane, room temperature electron mobility is dramatically increased. Mobility enhancements can be

incorporated into the basic MOSFET and basic CMOS inverter circuit in a number of ways as demonstrated by the many embodiments of this invention, but primarily through a semiconductor substrate material that allows for strained silicon surface channel PMOS and NMOS devices on the same common substrate materials. This strained silicon substrate allows for common semiconductor processing and semiconductor materials to be used.

In the basic strained silicon surface channel PMOS and NMOS structure, a compositionally graded SiGe buffer layer is used to accommodate the lattice mismatch between a relaxed SiGe layer and a Si substrate. By spreading the lattice mismatch over a distance, the SiGe graded buffer minimizes the number of dislocations reaching the surface and thus provides for a method of growing high-quality relaxed SiGe layers on a silicon substrate. After this, an epitaxially grown strained silicon layer is grown on the relaxed SiGe layer. Since the lattice constant of relaxed SiGe is larger than that of silicon, the strained silicon layer is under biaxial tension and thus the carriers exhibit strain-enhanced mobility.

Strained silicon surface channel devices can be fabricated with standard silicon CMOS processing tools and semiconductor materials. This compatibility allows for performance enhancement with no additional capital expenditures.

The strained silicon surface channel device technology is also scalable (shrinking size) using the standard silicon substrate based scaling tools (photolithography etc.) and materials (thinner gate oxide etc.). This scaling can be implemented for both long and short channel devices.

If desired, strained silicon surface channel substrates can be incorporated with SOI technology in order to provide ultra-high speed/low power circuits. Furthermore, strained silicon surface channel substrates can be incorporated with SiGe bonded wafers in order to provide ultra-high speed/low power circuits.

Since strained silicon surface channel technology is similar to bulk silicon technology, it can use other enhancement methods used for bulk silicon substrates (ion implantation, wiring etc.). As a result, strained silicon is an excellent technique for CMOS inverter circuit performance improvements.

Performance Characteristics

There are two primary methods of extracting performance enhancement from the increased carrier mobility, allowed for by strained silicon surface channel inverter circuits.

In the first method, the frequency of operation can be increased while keeping the

power constant. The propagation delay of a CMOS inverter is inversely proportional to the carrier mobility. Thus, if the carrier mobility is increased, as is the case with the strained silicon surface channel PMOS and NMOS CMOS inverter circuits, the propagation delay of the CMOS inverter circuit decreases, causing the overall CMOS inverter circuit speed to increase. This scenario is useful for applications such as desktop computers where the speed is more crucial than the power consumption.

In the second method, the power consumption can be decreased at a constant frequency of operation. When the carrier mobility increases, the gate voltage of the devices in the CMOS Inverter circuit can be reduced by an inverse amount while maintaining the same inverter speed of the CMOS inverter circuit. Since power is proportional to the square of the NMOS or PMOS device gate voltage of the CMOS inverter circuit, the reduction results in a significant decrease in the power consumption. This situation is most useful for portable applications that operate off of a limited power supply.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-section of the strained silicon substrate structure with a typical strained silicon surface channel MOSFET;

Figures 2A and 2B are graphs of mobility enhancements vs. effective Field for electrons and holes, respectively, for strained silicon on $Si_{1-x}Ge_x$ for x=10-30%;

Figure 3 is a table that displays surface roughness data for various relaxed SiGe buffers on Si substrates;

Figures 4A and 4B describes a schematic diagram of a CMOS inverter and its input and output voltage waveforms respectively;

Figures 5A-5C are schematic diagrams of the structures of a strained silicon MOSFET, a strained silicon MOSFET on SOI, and a strained silicon MOSFET on a bulk silicon substrate on bonded SiGe, respectively;

Figure 6 is a table showing electron and hole mobility enhancements measured for strained silicon on 20% and 30% SiGe;

Figure 7 is a table showing inverter characteristics for 1.2μm CMOS fabricated in both bulk and strained silicon when the interconnect capacitance is dominant;

Figure 8 is a table showing additional scenarios for strained silicon inverters when the interconnect capacitance is dominant;

Figure 9 is a table showing inverter characteristics for 1.2μm CMOS fabricated in both bulk and strained silicon when the device capacitance is dominant;

Figure 10 is a graph showing NMOSFET transconductance versus channel length

for various carrier mobilities;

Figure 11 is a graph showing the propagation delay of a 0.25μm CMOS inverter for a range of electron and hole mobility enhancements;

Figures 12A-12E show a fabrication process sequence for strained silicon on SOI substrates; and

Figures 13A-13C are circuit schematics for a NOR gate, a NAND gate and a XOR gate, respectively.

DETAILED DESCRIPTION OF THE INVENTION

Strained Silicon Surface Channel Devices

Figure 1 is a cross-section of the substrate structure 100 required to produce a strained silicon surface channel MOSFET. Polysilicon gate 112 is on top of thin silicon dioxide (SiO2) dielectric material 110, which is on top of biaxial strained silicon surface layer 108, which is on top of relaxed SiGe layer 106, which is on top of graded SiGe layer 102, which is on top of bulk silicon substrate layer 104. These layers are deposited using known, standard semiconductor processes.

The larger lattice constant, relaxed SiGe layer 106 applies biaxial strain to the silicon surface layer 108. In this structure, a compositionally SiGe graded buffer layer 102 is used to accommodate the lattice mismatch between a relaxed SiGe layer 106 and a silicon substrate 104. By spreading the lattice mismatch over a thickness of the SiGe graded buffer 102, the SiGe graded 102 buffer minimizes the number of *threading dislocations* (a dislocation comprised of a "line of atoms" not "lined up" with the crystallographic structure and which can cause electrical leakage) reaching the next layer to be deposited, which is the relaxed SiGe layer 106. This SiGe graded buffer 102 provides a means for growing high quality relaxed SiGe layer 106 on silicon substrate 104.

Subsequently, a strained silicon surface layer 108 below the critical thickness (the thickness where it becomes energetically favorable to introduce dislocations) can be grown on the relaxed SiGe layer 106. Since the lattice constant of relaxed SiGe layer 106 is larger than that of the silicon substrate 104, the strained silicon surface layer 108 is under biaxial tension 150 (tension in both axes 160 and 170) and thus the carriers exhibit strain-enhanced mobility.

In the structure shown in Figure 1, the strained silicon surface layer 108 is placed under biaxial tension by the underlying, larger lattice constant SiGe layer. From a *solid*

state physics point of view, it is well known in the art that the strain of the silicon layer causes the conduction band of the silicon layer to split into two-fold and four-fold degenerate bands. The two-fold band is preferentially occupied since it sits at a lower energy state. The energy separation between the bands is approximately

$$\Delta E_{strain} = 0.67 \cdot x \text{ (eV)} \quad (1)$$

where x is equal to the Ge content in the SiGe layer. The equation shows that the band splitting increases as the Ge content increases. This splitting causes mobility enhancement by two mechanisms. First, the two-fold band has a lower effective mass, and thus higher mobility than the four-fold band. Therefore, as the higher mobility band becomes energetically preferred, the average carrier mobility increases. Second, since the carriers are occupying two orbitals instead of six, and therefore inter-valley phonon scattering is reduced, further enhancing the carrier mobility.

The effects of germanium (Ge) concentration (amount of germanium in silicon) of the Ge in the relaxed SiGe layer 106 in Figure 1, on the electron and hole mobility of the surface channel silicon devices can be seen in Figures 2A and 2B, respectively. Figures 2A and 2B are graphs of mobility enhancements versus effective fields in megavolts per centimeter for electrons and holes, respectively, for strained silicon on $Si_{1-x}Ge_x$ for x=10-30%. At 20% Ge, the electron enhancement at high fields is approximately 1.75 (relative to bulk silicon) while the hole enhancement is essentially negligible. Above approximately 20% Ge, the electron enhancement saturates (no longer increases for increased Ge concentrations). This saturation occurs because the conduction band splitting is large enough that almost all of the electrons occupy the high mobility band. As shown in Figure 2B, hole enhancement saturation has not yet been observed; therefore, raising the Ge concentration to 30% increases hole mobility by a factor of 1.4. Hole enhancement saturation is predicted to occur at a Ge concentration of about 40%. The ability to add more Ge to increase the hole mobility without further increases in electron mobility will become useful in designing surface channel CMOS inverter designs.

Researchers have found that at significant increases in percent Ge content in the SiGe layer, the surface roughness of the SiGe layer increases and becomes problematic (e.g., it is hard to do submicron photolithography on it). Because of this, researchers have chosen to use low percentages of Ge in the SiGe layer so that surface roughness effects are minimized and thus see only the benefit of the electron mobility. In this case, researchers do not see the enhancement of hole mobility achieved at higher percentages of Ge. The low

hole mobility in surface channel devices has caused other researchers to move to higher mobility, buried channel devices for the PMOSFETs.

Until recently, the material quality of relaxed SiGe on Si was insufficient for utilization in CMOS fabrication. During epitaxial growth, the surface of the SiGe becomes very rough and creates crosshatched patterns on the surface of the SiGe layer, which causes further problems with subsequent photolithography as well as device degradation since the gate oxide is grown on this surface. This roughness is caused because the SiGe material on Si is relaxed via dislocation introduction. Researchers have tried to control the surface morphology through the growth process. However, since the stress fields from the misfit dislocations affect the growth front, no intrinsic epitaxial solution is possible. U.S. Pat. No. 6,107,653 issued to Fitzgerald, incorporated herein by reference, describes a method of planarization and regrowth that allows all devices on relaxed SiGe to possess a significantly flatter surface. This reduction in surface roughness is critical in the production of strained Si CMOS devices since it increases the yield for fine-line lithography.

Figure 3 is a table that displays surface roughness data for various relaxed SiGe buffers on Si substrates. It will be appreciated that the as-grown crosshatch pattern for relaxed $Si_{0.8}Ge_{0.2}$ buffers creates a typical roughness of approximately 7.9nm. This average roughness increases as the Ge content in the relaxed buffer is increased. Thus, for any relaxed SiGe layer that is relaxed through dislocation introduction during growth, the surface roughness is unacceptable for state-of-the-art photolithography. After the relaxed SiGe is planarized, the average roughness is less than 1nm (typically 0.57nm), and after a 1.5μm silicon device layer epitaxial grown layer is completed, the average roughness is 0.77nm. Therefore, after the complete structure is fabricated, there is over an order of magnitude reduction in the surface roughness. The resulting high quality material is well suited for state of the art CMOS photolithographic processing.

It is shown that because of the planarized SiGe layer, we can use higher Ge percentages so that the strained silicon provides significant CMOS enhancement since both high electron and high hole mobility can be achieved using surface channel devices for both NMOS and PMOS respectively without the need for a buried channel. This design allows for high performance without the complications of adding a buried channel device to obtain dual channel operation and without adding complexity to circuit fabrication (surface and buried channel devices on the same substrate).

CMOS Inverter

Figure 4A is a schematic diagram of a CMOS inverter 400. When the input voltage, 401 or V_{in}, to the inverter is low, a PMOS transistor 402 turns on, charges up a load capacitance 404, and the output 420 goes to a gate drive 406, V_{DD}. Alternatively, when 401 V_{in} is high, an NMOS transistor 408 turns on, and discharges the load capacitance 404, and the output node goes to ground level 410. In this manner, the inverter is able to perform the logic swing necessary for digital processing.

The propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the load capacitance 404 or C_L through PMOS 402 and NMOS 408 transistors, respectively. The load capacitance, denoted as 404 or C_L, represents a lumped model of all of the capacitances between V_{out} 420 and ground 410.

Lumped Capacitance

The following equation defines the Lumped Capacitance:

$$C_L = (C_{dp1} + C_{dn1}) + (C_{gp2} + C_{gn2}) + C_w \quad (2)$$

where C_{dp1} and C_{dn1} are the equivalent drain diffusions capacitances of PMOS 402 and NMOS 408 transistors, respectively, of the first inverter, while C_{gp2} and C_{gn2} are the gate capacitances of the an attached second gate inverter (not shown). C_w represents the wiring capacitance. This is explained by reference #1 to *Chapter 3 of Digital Integrated Circuits by Jan Rabaey, Prentice Hall Electronics and VLSI series, copyright 1996.*

Time Constant

Figure 4B shows the propagation delay of the CMOS inverter of Figure 4B. The gate defines how quickly it responds to a change at its input and relates directly to the speed and performance metrics. The propagation delay expresses the delay experienced by a signal passing through the gate. It is measured between the 50% transition points of the input and output waveforms, as shown in Figure 4A for the inverting gate. Because the gate displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary. The t_{pLH} defines the response time of the gate for a low to high (or positive) output transition, while t_{pHL} refers to a high to low (or negative) transition. The overall propagation delay is defined as the average of the two:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

(3)

Since the load capacitance must be fully charged or discharged before the logic swing is complete, the magnitude of C_L has a large impact on inverter performance. The performance is usually quantified by two variables: the propagation delay, t_p, and the power consumed, P. The propagation delay is defined as how quickly a gate responds to a change in its input and can also be given by:

$$t_p = \frac{C_L \cdot V_{DD}}{I_{av}} \qquad (4)$$

where I_{av} is the average current during the voltage transition. There is a propagation delay term associated with the NMOS discharging current, t_{pHL}, and a term associated with the PMOS charging current, t_{pLH}. The average of these two values (as before) represents the overall inverter delay:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

(4)

Power

Assuming that static and short-circuit power are negligible, the power consumed can be written as

$$P = \frac{C_L \cdot V_{DD}^2}{t_p} \qquad (5)$$

From equations above, one can see that both the propagation delay and the power consumption have a linear dependence on the load capacitance. In an inverter, C_L consists of two major components: wiring capacitance and device capacitance. Which component dominates C_L depends on the architecture of the circuit in question.

Mobility – μ_n or μ_p

The electron velocity is related to the electric field through a parameter called the mobility of the M material (μ_n)or the mobility of the P material (μ_p) (expressed in cm^2/V-sec). The mobility is a complex function of the crystal structure. The higher the mobility, the greater the electron velocity.

Gain factor – k_n or k_p

According to reference #1, the gain factor is a product of process transconductance and the dimensions width/length (W/L) of the transistor. The propagation delay of a gate can be minimized by increasing k_n or k_p, or equivalently, increase the W/L ratio of the transistors. This might seem a straightforward and desirable solution. However, a word of caution is necessary. Increasing the W/L ratio (transistor size) also increases the diffusion capacitance (and C_L) as well as the gate capacitance. An equation for gain factor is shown below:

$$K_n = \mu_n C_{ox} \times \frac{\mu_n}{L_n} \qquad (6)$$

where C_{ox} is the capacitance of the thin oxide gate capacitance.

Derivation of relationship between t_p, C_L, μ, and W/L:

In order to understand the inverter performance of propagation delay (t_p) and power (P), it is necessary to derive t_p and P in terms of μ_n, μ_p, W, L, and C_L so that we can see the effects of these design parameters. From reference #1, it is known that:

$$t_p = \frac{C_L}{2V_{DD}K_n}\left(1 + \frac{\mu_n}{\mu_p}\left(\frac{W_n}{L_n}\right)\frac{L_p}{W_p}\right) \qquad (7)$$

where V_{DD} is the gate drive voltage.

Substituting gain factor as shown in equation 6,

$$t_p = \frac{C_L}{2V_{DD}\mu_n C_{ox}} \times \frac{L_n}{W_n}\left(1+\frac{\mu_n}{\mu_p}\left(\frac{W_n}{L_n}\right)\frac{L_p}{W_p}\right) \quad (8)$$

therefore:

$$t_p = \frac{C_L}{2V_{DD}\mu_n C_{ox}}\left(\frac{L_n}{W_n}+\frac{\mu_n}{\mu_p}\times\frac{L_p}{W_p}\right) \quad (9)$$

and further,

$$t_p = \frac{C_L}{2V_{DD}C_{ox}}\left(\frac{L_n}{\mu_n W_n}+\frac{L_p}{\mu_p W_p}\right) \quad (10)$$

therefore from equation 7, the following relationships can be defined:

$$t_p \propto C_L \propto \frac{1}{\mu_n} \propto \frac{1}{\mu_p} \propto \frac{1}{W_n} \propto \frac{1}{W_p} \quad (11)$$

Derivation of relationship between P and W/L

Assuming that static and short-circuit power are negligible, the power equation (5) and (11) above we know t_p is inversely proportional to W. Therefore it is derived that:

$$P \propto W \quad (12)$$

which means that as width decreases, so does the power of the circuit.

First Embodiment : Basic Surface Channel PMOS and NMOS Strained Silicon Devices Forming an Inverter Circuit

Figures 5A is a basic schematic diagram of the MOSFET device structures of a strained silicon MOSFET 500 on a bulk silicon substrate. The structure in Figure 5A contains silicon substrate 504, with a layer of a SiGe graded buffer 502 grown on it, which in turn has a relaxed SiGe layer 506 grown on it, which in turn has a strained silicon layer 508 grown on it. These layers are grown through standard semiconductor epitaxial processing. As would be standard to semiconductor processing, the MOSFET and the isolation regions are also defined. These are shown in Figure 5A as shallow trench isolations regions 516, gate oxide region 510, polysilicon gate region 512, and lightly doped drain region 514 and lightly doped source region 513. These are the basic regions of a MOSFET device. It should be noted that this device can be defined as either an N-type channel or P-type channel through appropriate and well-understood semiconductor ion implantation of dopants as well as their subsequent anneals. Also shown in Figure 5A are the thicknesses of graded SiGe layers 502 (typically 1-5 microns), relaxed SiGe layer 506 (typically 0.1-2 microns), strained silicon layer 508 (typically less than 300 angstroms or approximately equal to or less than the critical thickness), and gate oxide 510 (typically 100 angstroms). Also shown in Figure 5A are source connection 521, gate connection 522 and drain connection 523. It should be noted that planarization of the SiGe layers may be required to reduce surface roughness.

In the MOSFET structure in Figure 5A, the strained Si layer 508 serves as the carrier channel, thus enabling improved device performance over their bulk Si counterparts.

Once the NMOS and PMOS are defined in the semiconductor process (using standard techniques known in the art), the wiring connections of the NMOS and PMOS devices are connected as shown in the inverter circuit of Figure 4A. Thus a strained silicon surface channel inverter is formed, allowing the benefits of high percent Ge and hence both high electron and high hole mobility.

Second Embodiment : Basic Surface Channel PMOS and NMOS Strained Silicon Devices Forming an Inverter Circuit Using Bonded SOI

Figure 5B is a basic schematic diagram of the MOSFET device structures of a strained silicon MOSFET 550 on a bulk silicon substrate on Silicon On Insulator (SOI). The structure in Figure 5B contains silicon substrate 554, with a layer of a SOI 552 bonded to it. This bonded SOI was previously formed with a relaxed SiGe layer 556 grown on it, which in turn has a strained silicon layer 558 grown on it. These layers on the SOI are

grown through standard semiconductor epitaxial processing. The MOSFET and the isolation regions are also defined according to standard semiconductor processing. These basic regions of a MOSFET device are shown in Figure 5B as shallow trench isolations regions 566, gate oxide region 560, polysilicon gate region 562, and lightly doped drain region 564 and lightly doped source region 563. . It should be noted that this device can be defined as either an N-type channel or P-type channel through appropriate and well-understood semiconductor ion implantation of dopants as well as their subsequent anneals. Also shown in Figure 5B are source connection 571, gate connection 572 and drain connection 573. In the MOSFET structure in Figure 5B, the strained Si layer 558 serves as the carrier channel, thus enabling improved device performance over their bulk Si counterparts.

Strained silicon technology can also be incorporated with SOI technology for added performance benefits. Figures 12A-12E show a fabrication process sequence for strained silicon on SOI substrates. First, a SiGe graded buffer layer 1202 is grown on a silicon substrate 1200 with a uniform relaxed SiGe cap layer 1204 of the desired concentration (Figure 12A). This wafer is then bonded to a silicon wafer 1206 oxidized with a SiO_2 layer 1208 (Figures 12B-12C). The initial substrate and graded layer are then removed through either wafer thinning or delamination methods. The resulting structure is a fully relaxed SiGe layer on oxide (Figure 12D). A strained silicon layer 1210 can subsequently be grown on the engineered substrate to provide a platform for strained silicon, SOI devices (Figure 12E). The resulting circuits would experience the performance enhancement of strained silicon as well as about an 18% performance improvement from the SOI architecture. In short channel devices, this improvement is equivalent to 3-4 scaling generations at a constant gate length.

Once the NMOS and PMOS are defined in the semiconductor process (using standard techniques known in the art), the wiring connections of the NMOS and PMOS devices are connected as shown in the inverter circuit of Figure 4A. Thus a strained silicon surface channel inverter is formed, allowing the benefits of high percent Ge and hence both high electron and high hole mobility.

Third Embodiment: Basic Surface Channel PMOS and NMOS Strained Silicon Devices Forming an Inverter Circuit Using Bonded SiGe

Figures 5C is a basic schematic diagram of the MOSFET device structures of a strained silicon MOSFET 570 on a bulk silicon substrate on bonded SiGe. The structure in

Figure 5C contains a silicon substrate 574. A relaxed SiGe layer 576 is bonded to substrate 574. On top of this relaxed SiGe 576 layer is a strained silicon layer 578, which in turn has a layer of SiO2 580 on top of it. On top of SiO2 580 is polysilicon gate region 582. The MOSFET and the isolation regions are also defined according to standard semiconductor processing. These basic regions of a MOSFET device are shown in Figure 5C as shallow trench isolations regions 586, gate oxide region 580, polysilicon gate region 582, and lightly doped drain region 584 and lightly doped source region 583. It should be noted that this device can be defined as either an N-type channel or P-type channel through appropriate and well-understood semiconductor ion implantation of dopants as well as their subsequent anneals. Also shown in Figure 5C are source connection 591, gate connection 592 and drain connection 593.

A similar fabrication method can be used to provide relaxed SiGe layers directly on Si, i.e., without the presence of the graded buffer or an intermediate oxide. This heterostructure is fabricated using the sequence shown in Figures 12A-12D without the oxide layer on the Si substrate. The graded composition layer possesses many dislocations and is quite thick relative to other epitaxial layers and to typical step-heights in CMOS. In addition, SiGe does not transfer heat as rapidly as Si. Therefore, a relaxed SiGe layer directly on Si is well suited for high power applications since the heat can be conducted away from the SiGe layer more efficiently.

Once the NMOS and PMOS are defined in the semiconductor process using standard techniques known in the art, the wiring connects the NMOS and PMOS device together as an inverter as shown in Figure 4A. Thus a strained silicon surface channel inverter is formed.

Fourth Embodiment: PMOS and NMOS Surface Channel Strained Silicon Devices Forming an Inverter Circuit with Optimized SiGe Ratios of the Relaxed SiGe Layer for Enhanced Speed with Lower V_{DD}, Constant Power and Device Capacitance Much Greater than Wiring Capacitance.

Whether the basic inverter devices are built on bulk silicon as in Figure 5A or on bonded SOI as in Figure 5B, or on bonded SiGe as in Figure 5C, the Ge percentage used in the relaxed SiGe can be modified to create the strained silicon layer, circuit speed, or circuit power effects. When strained silicon is used as the carrier channel, the electron and hole mobilities are multiplied by enhancement factors. As discussed before in Figures 2A and

2B, the enhancement differs for electrons and holes and also varies with the Ge fraction in the underlying SiGe layer. A summary of the enhancements for $Si_{0.8}Ge_{0.2}$ and $Si_{0.7}Ge_{0.3}$ is shown in Figure 6. Figure 6 is a table showing electron and hole mobility enhancements measured for strained silicon on 20% and 30% SiGe. As will be shown by both derivations from first principles and by calculations in a MatLab™ analysis tool, we can enhance the speed of a basic inverter by using relaxed SiGe and more importantly, with addition of the right amount of Ge in the relaxed SiGe layer, the strained silicon layer on top of this layer will produce optimized inverter speeds over bulk silicon surface channel devices commonly used in inverters today.

If we consider the mobility of the NMOS and PMOS for bulk silicon devices (μ_n or μ_p) to be a reference of unity (1), then the use of strained silicon on relaxed SiGe as described in Figure 6 (using the enhancement factor for each device) demonstrates mobility $\mu_n = 1.75$, $\mu_p = 1$ for 20% Ge in relaxed SiGe; or mobility $\mu_n = 1.8$, $\mu_p = 1.4$ for 30% Ge in relaxed SiGe. Both μ_n and μ_p are both increased for 30% Ge and only μ_n is enhanced for 20% Ge.

From equation 10, which is derived from first principles of an inverter for MOSFETs:

$$t_p = \frac{C_L}{2V_{DD}C_{ox}}\left(\frac{L_n}{\mu_n W_n} + \frac{L_p}{\mu_p W_p}\right) \qquad (10)$$

if we hold constant the device size($\mathbf{W_n}$, $\mathbf{W_p}$, $\mathbf{L_n}$, $\mathbf{L_p}$) for bulk silicon to be the same as for our strained silicon, it can be seen that when either μ_n or μ_p go up, the t_p goes down and hence the inverter gets faster.

These enhancements are shown using results from a MatLab™ analysis tool where these parameters are programmed to calculate more exacting results. We have chosen a nominal design point of sizes of the basic devices of an inverter to demonstrate the enhancement of speed. We have incorporated a ground rule of a 1.2μm CMOS model in order to quantify the effects on inverter performance. The analysis minimized the wiring capacitance so that Cw was much less than the lumped device capacitance of equation (2), so only device effects were investigated.

The values for a bulk silicon, 1.2μm symmetrical inverter are calculated and are shown in Figure 7. In this set of calculations, the device capacitance is much greater than the wiring capacitance. Figure 7 is a table showing inverter characteristics for 1.2μm CMOS fabricated in both bulk and strained silicon. The propagation delay for the bulk silicon inverter is t_p = 203.5 picoseconds and the consumed power is 3.93mW. In an application where speed is paramount, such as in desktop computing, strained silicon provides a good way to enhance the circuit speed. Assuming no change from the bulk silicon design, a strained silicon inverter on $Si_{0.8}Ge_{0.2}$ results in a 15.1% speed increase over the bulk silicon base case at constant power. When the channel is on $Si_{0.7}Ge_{0.3}$, the speed enhancement improves to 29.3% over the bulk silicon base case (Figure 7).

If there is no change from the bulk silicon design, a PMOS and NMOS surface channel strained silicon inverter circuit will achieve higher speeds over the bulk silicon. If strained silicon were simply swapped in the process for the substrate, outside of taking into account the changes needed in processing to ensure the implants and other processes created the same inverter, attached circuits may have to be modified to eliminate race conditions that may occur. That is, if inverters were sped up, the circuits that attach to these inverters may have to be modified in terms of changes there lengths or widths to account for the enhanced speeds. Note that V_{DD} was reduced to maintain a constant power.

Fifth Embodiment : PMOS and NMOS Surface Channel Strained Silicon Devices Forming an Inverter Circuit with optimized SiGe ratios of the Relaxed SiGe layer for enhanced Speed by maintaining V_{DD} for Wiring Capacitance Much Greater Than Device Capacitance

In advanced ground rule designs, wiring limitations force designers to pack wires in much greater density and even at times create "borderless contacts" (where the diffusion contact overlaps but is insulated from the gate) between the source diffusion region or drain diffusion region and the gate. When this and other wiring enhancements are made, wiring capacitance becomes dominant over device capacitance.

As described in the fourth embodiment above, a further enhancement is found by maintaining V_{DD} for wiring capacitance-dominated designs. As shown in Figure 8 (where the wiring capacitance is much greater than device capacitance) and when V_{DD} is held constant (5 volts) at the same amount over the bulk silicon base case, the enhancement of speed increases to 22.3% over the bulk silicon base case and 36.7%, for Si on $Si_{0.8}Ge_{0.2}$ and $Si_{0.7}Ge_{0.3}$, respectively. Note that in both these cases more power is required to achieve this speed (-28.0% and -58.2% power reduction over the bulk silicon base case, respectively).

Sixth Embodiment : PMOS and NMOS Surface Channel Strained Silicon Devices Forming an Inverter Circuit with optimized SiGe ratios of the Relaxed SiGe Layer for Enhanced Power by Reducing V_{DD} for Device Capacitance Dominated Circuits.

As will be shown by both derivations from first principles and by calculations in a MatLab™ analysis tool, we can enhance the power of a basic inverter circuit by using a strained silicon surface channel for both PMOS and NMOS and more importantly, with the addition of the right amount of Ge in the relaxed SiGe layer, the strained silicon layer on top of this layer will produce optimized inverter power over bulk silicon surface channel devices used in inverters today.

If we consider the mobility of the NMOS and PMOS for bulk silicon devices (μ_n or μ_p) to be a reference of unity or 1, then the use of strained silicon on relaxed SiGe as described in Figure 6 (using the enhancement factor for each device) demonstrates mobility $\mu_n = 1.75$, $\mu_p = 1$ for bulk silicon for 20% Ge in relaxed SiGe; or mobility $\mu_n = 1.8$, $\mu_p = 1.4$ for that of bulk silicon for 30% Ge in relaxed SiGe. Both μ_n and μ_p are both increased for 30% Ge and only μ_n is enhanced for 20% Ge.

From equation 10, which is derived from first principles of an inverter for MOSFETs:

$$t_p = \frac{C_L}{2V_{DD}C_{ox}}\left(\frac{L_n}{\mu_n W_n} + \frac{L_p}{\mu_p W_p}\right) \quad (10)$$

if we hold constant the device size($\mathbf{W_n}$, $\mathbf{W_p}$, $\mathbf{L_n}$, $\mathbf{L_p}$) for bulk silicon to be the same as for our strained silicon, it can be seen that when either μ_n or μ_p go up, the t_p goes down and hence the in the inverter gets faster.

Also, from equation (5) before, we can see that:

$$P = \frac{C_L \cdot V_{DD}^{\ 2}}{t_p} \qquad (5)$$

Power can be enhanced by the square of V_{DD} (which is the drain voltage of the inverter) as well as a decrease in $\mathbf{t_p}$. So by adding strained silicon the power goes up since $\mathbf{t_p}$ goes down and when can decrease V_{DD} to further reduce power. Because we have used strained silicon as a substrate we can actually reduce V_{DD} to reduce power while maintaining the speed.

As shown in Figure 7, by reducing the gate drive, V_{DD}, the power is reduced at a constant speed. For 20% SiGe, the power consumption is 27% lower than its bulk silicon counterpart. When 30% SiGe is used, the power is reduced by 43.7% from the bulk silicon value. This power reduction is important for portable computing applications such as laptops and handhelds.

Seventh Embodiment: PMOS and NMOS Surface Channel Strained Silicon Devices Forming an Inverter Circuit With Optimized SiGe Ratios Of The Relaxed SiGe Layer For Enhanced Density.

As will be shown by derivations from first principles, we can reduce the density or size of an inverter circuit and maintain power and speed by using relaxed SiGe and more importantly, with addition of the right amount of Ge in the relaxed SiGe layer, the strained silicon layer on top of this layer will produce optimized inverter density over the bulk silicon surface channel devices used in inverters today.

If we consider the mobility of the NMOS and PMOS for bulk silicon devices (μ_n or μ_p) to be a reference of unity or 1, then the use of strained silicon on relaxed SiGe or mobility ratio as shown in Figure 6 (using the enhancement factor for each device) demonstrates mobility $\mu_n = 1.75$ and $\mu_p = 1$ for 20% Ge in relaxed SiGe; or mobility $\mu_n = 1.8$ and $\mu_p = 1.4$ for 30% Ge in relaxed SiGe. Both $\mu_{n \text{ and }} \mu_p$ are both increased for 30% Ge and only μ_n is enhanced for 20% Ge.

From equation 10, which is derived from first principles of an inverter for MOSFET's,

$$t_p = \frac{C_L}{2V_{DD}C_{ox}}\left(\frac{L_n}{\mu_n W_n} + \frac{L_p}{\mu_p W_p}\right) \qquad (10)$$

Since both μ_n and μ_p (or at least μ_n) goes up, we see that t_p goes down for a faster inverter. We can raise the t_p back up to where it may be for bulk silicon, by reducing W_n and W_p, in other words, we can reduce W_n and W_p by the factor that μ_n and μ_p increased so that the $\mu_n W_n$ and $\mu_p W_p$ factor remains constant. Thus, for the same speed t_p, PMOS and NMOS strained silicon surface channel devices in an inverter circuit allows us to reduce the size of the inverter, everything else being held constant.

Eighth Embodiment: PMOS and NMOS Surface Channel Strained Silicon Devices in a *Symmetric* Inverter Circuit with Optimized SiGe Ratios of the Relaxed SiGe Where Wiring Capacitance Dominant Circuits.

One drawback of strained silicon, surface channel CMOS is that the electron and hole mobility's are unbalanced further by the uneven electron and hole enhancements. This unbalance in mobility translates to an unbalance in the noise margins of the inverter. *The noise margin represents the levels of noise that can be sustained when the gates are cascaded. A measure of the sensitivity of a gate to noise is given by the noise margin NM_L (noise margin low) and NM_H (noise margin high) which quantize the legal "0" and "1" of digital circuits. (Further explanation of these noise margins can be found in reference #1, Chapter 3 of Digital Integrated Circuits by Jan Rabaey, Prentice Hall Electronics and VLSI series, copyright 1996.)* The noise margins represent the allowable variability in the high and low inputs to the inverter.

In bulk advanced ground rules where wiring capacitance is dominant, both the low and high noise margins are unbalanced for strained silicon at either 20% or 30% SiGe. For example, non-symmetric circuit (NM_L) in Figure 8 shows that the high noise margin, NM_H for 20% Ge is 2.37 volts when the low noise margin is 1.75 volts. Also shown is non-symmetric circuit in Figure 8 for 30% Ge. In this case, the high noise margin is 2.2 volts and the low noise margin is 1.92 volts.

However, if a symmetrical inverter is required, the PMOS device width must be increased to μ_n/μ_p times the NMOS device width. This translates to a 75% increase in PMOS width (1.75 x 5.4 = 9.45) for $Si_{0.8}Ge_{0.2}$, and a 29% increase (1.29 x 5.4 = 6.94) over the bulk silicon base case for $Si_{0.7}Ge_{0.3}$. If the increased area is acceptable for the intended application, inverter performance can be further enhanced. As shown in Figure 8, in the constant power scenario, the speed can now be increased by 23.0% for $Si_{0.8}Ge_{0.2}$ and by 33.8% for $Si_{0.7}Ge_{0.3}$ for a symmetric inverter over the bulk silicon base case. When the power is reduced for a constant frequency, a 37.6% and 47.0% reduction in consumed power is possible with 20% and 30% SiGe, respectively (Figure 8). However, in many applications an increase in device area is not tolerable. In these situations, if inverter symmetry is required, it is best to use strained silicon of 30% SiGe. Since the electron and hole enhancement is comparable on $Si_{0.7}Ge_{0.3}$, it is easier to trade off size for symmetry to meet the needs of the application.

Ninth Embodiment : PMOS and NMOS Surface Channel Strained Silicon Devices in a *Optimized Design* Inverter with Optimized SiGe Ratios of the Relaxed SiGe and Dominated by Device Capacitance.

The device capacitance is dominant over the wiring capacitance in many analog applications. The device capacitance includes the diffusion and gate capacitance of the inverter itself as well as all inverters connected to the gate output, known as the fan-out. Since the capacitance of a device depends on its area, PMOS upsizing results in an increase in C_L. If inverter symmetry is not a prime concern, reducing the PMOS device size can increase the inverter speed. This PMOS downsizing has a negative effect on t_{pLH} but has a positive effect on t_{pHL}. The optimum speed is achieved when the ratio between PMOS and NMOS widths is set to $\sqrt{\mu_n / \mu_p}$, where μ_n and μ_p represent the electron and hole mobility, respectively.

Figure 9 is a table showing inverter characteristics for 1.2μm CMOS fabricated in both bulk and strained silicon when the device capacitance is dominant. The strained silicon inverters are optimized to provide high speed at constant power and low power at constant speed. For strained silicon on $Si_{0.8}Ge_{0.2}$, the electron mobility is higher than the hole mobility. When the PMOS width is re-optimized by adjusting W_p and V_{DD} to

accommodate these mobilities, i.e., by using the $\sqrt{\mu_n / \mu_p}$ optimization (see Reference #1), the strained silicon PMOS device on $Si_{0.8}Ge_{0.2}$ is over 30% wider ((4.12 – 3.11)/3.11) than the bulk Si PMOS device. The resulting increase in capacitance offsets some of the advantages of the enhanced mobility. Therefore, only a 4% speed increase occurs at constant power, and only an 8% decrease in power occurs at constant speed over the bulk silicon base case.

Although these improvements are significant, they represent a fraction of the performance improvement seen with a generation of scaling and do not surpass the performance capabilities available with SOI architectures.

In contrast, strained silicon on $Si_{0.7}Ge_{0.3}$ offers a significant performance enhancement at constant gate length for circuits designed to the $\sqrt{\mu_n / \mu_p}$ optimization. Since the electron and hole mobilities are more balanced, the effect on the load capacitance is less substantial. As a result, large performance gains can be achieved. At constant power, the inverter speed can be increased by over 23% and at constant speed, the power can be reduced by over 37% over the bulk silicon base case. The latter enhancement has large implications for portable analog applications such as wireless communications.

As in the microprocessor case (wiring or interconnect capacitance dominated), the strained silicon devices suffer from small low noise margins. Once again, this effect can be minimized by using 30% SiGe. If larger margins are required, the PMOS device width can be increased to provide the required symmetry. However, this PMOS upsizing increases C_L and thus causes an associated reduction in performance. Inverter design must be tuned to meet the specific needs of the intended application.

Tenth Embodiment : Strained Silicon Devices in an Inverter with optimized SiGe ratios of the Relaxed SiGe for short and long channel devices.

In short channel devices, the lateral electric field driving the current from the source to the drain becomes very high. As a result, the electron velocity approaches a limiting value called the saturation velocity, v_{sat}. Since strained silicon provides only a small enhancement in v_{sat} over bulk silicon, researchers believed that strained silicon would not provide a performance enhancement in short channel devices. However, recent data shows

that transconductance values in short channel devices exceed the maximum value predicted by velocity saturation theories. Figure 10 is a graph showing NMOSFET transconductance versus channel length for various carrier mobilities. The dashed line indicates the maximum transconductance predicted by velocity saturation theories. The graph shows that high low-field mobilities translate to high high-field mobilities. The physical mechanism for this phenomenon is still not completely understood; however, it demonstrates that short channel mobility enhancement can occur in strained silicon.

The power consumed in an inverter depends on both V_{DD} and t_p. Therefore, as t_p is decreased due to mobility enhancement, V_{DD} must also be decreased in order to maintain the same power consumption. In a long channel device, the average current, I_{av}, is proportional to V_{DD}^2. Inserting this dependence into equation 3 reveals an inverse dependence of the propagation delay on V_{DD}. Thus, as the average current in strained silicon is increased due to mobility enhancement, the effect on the propagation delay is somewhat offset by the reduction in V_{DD}.

A comparison of the high-speed scenario device dominated capacitance inverter circuit shown in Figure 7 to the constant V_{DD} scenario wiring capacitance dominated inverter circuit shown in Figure 8 reveals the effect the reduced V_{DD} has on speed enhancement. In a short channel device, the average current is proportional to V_{DD} not V_{DD}^2, causing the propagation delay to have no dependence on V_{DD} (assuming $V_{DD}>>V_T$). As a result, mobility enhancements in a short channel, strained silicon inverter are directly transferred to a reduction in t_p. A 1.2μm strained silicon inverter on 30% SiGe experiences a 29.3% increase in device speed for the same power (Figure 7).

Figure 11 is a graph showing the propagation delay of a short channel 0.25μm CMOS inverter for a range of electron and hole mobility enhancements. Although the exact enhancements in a short channel device vary with the fabrication processes, Figure 11 demonstrates that even small enhancements can result in a significant effect on t_p.

Eleventh Embodiment : Strained Silicon Devices in an Other Digital Gates with optimized SiGe ratios of the Relaxed SiGe.

Although the preceding embodiments describe the performance of a CMOS inverter,

strained silicon enhancement can be extended to other digital gates such as NOR, NAND, and XOR structures. Circuit schematics for a NOR gate 1300, a NAND gate 1302 and a XOR gate 1304 are shown in Figures 13A-C, respectively. The optimization procedures are similar to that used for the inverter in that the power consumption and/or propagation delay must be minimized while satisfying the noise margin and area requirements of the application. When analyzing these more complex circuits, the operation speed is determined by the worst-case delay for all of the possible inputs.

For example, in the pull down network of the NOR gate 1300 shown in Figure 13A, the worst delay occurs when only one NMOS transistor is activated. Since the resistances are wired in parallel, turning on the second transistor only serves to reduce the delay of the network. Once the worst-case delay is determined for both the high to low and low to high transitions, techniques similar to those applied to the inverter can be used to determine the optimum design.

The enhancement provided by strained silicon is particularly beneficial for NAND-only architectures. As shown in Figure 13B, in the architecture of the NAND gate 1302, the NMOS devices are wired in series while the PMOS devices are wired in parallel. This configuration results in a high output when either input A or input B is low, and a low output when both input A and input B are high, thus providing a NAND logic function. Since the NMOS devices are in series in the pull down network, the NMOS resistance is equal to two times the device resistance. As a result, the NMOS gate width must be doubled to make the high to low transition equal to the low to high transition.

Since electrons experience a larger enhancement than holes in strained Si, the NMOS gate width up scaling required in NAND-only architectures is less severe. For 1.2μm strained silicon CMOS on a $Si_{0.8}Ge_{0.2}$ platform, the NMOS gate width must only be increased by 14% to balance the pull down and pull up networks (assuming the enhancements shown in Figure 6). Correspondingly, for 1.2μm CMOS on $Si_{0.7}Ge_{0.3}$, the NMOS width must be increased by 55% since the n and p enhancements are more balanced. The high electron mobility becomes even more important when there are more than two inputs to the NAND gate, since additional series-wired NMOS devices are required.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. A CMOS inverter comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer; and

a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

2. The CMOS inverter of claim 1, wherein the heterostructure further comprises a planarized surface positioned between the strained surface layer and the Si substrate

3. The CMOS inverter of claim 1, wherein the surface roughness of the strained surface layer is less than 1nm

4. The CMOS inverter of claim 1, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate

5. The CMOS inverter of claim 1, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate

6. The CMOS inverter of claim 1, wherein the strained surface layer comprises Si

7. The CMOS inverter of claim 1, wherein $0.1<x<0.5$

8. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in bulk silicon.

9. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in the strained surface layer.

10. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in bulk silicon.

11. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of

the ratio of the electron mobility and the hole mobility in the strained surface layer.

12. The CMOS inverter of claim 7, wherein the gate drive is reduced to lower power consumption.

13. In a high speed integrated circuit, the CMOS inverter of claim 7.

14. In a low power integrated circuit, the CMOS inverter of claim 7

15. An integrated circuit comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained layer on said relaxed $Si_{1-x}Ge_x$ layer; and

a p transistor and an n transistor formed in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and said p transistor are interconnected in a CMOS circuit.

16. The integrated circuit of claim 15, wherein the heterostructure further comprises a planarized surface positioned between the strained layer and the Si substrate.

17. The integrated circuit of claim 15, wherein the surface roughness of the strained layer is less than 1nm.

18. The integrated circuit of claim 15, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

19. The integrated circuit of claim 15, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate

20. The integrated circuit of claim 15, wherein the strained layer comprises Si.

21. The integrated circuit of claim 15, wherein $0.1<x<0.5$

22. The integrated circuit of claim 15, wherein the CMOS circuit comprises a logic gate.

23. The integrated circuit of claim 15, wherein the CMOS circuit comprises a NOR

gate

24. The integrated circuit of claim 15, wherein the CMOS circuit comprises an XOR gate.

25. The integrated circuit of claim 15, wherein the CMOS circuit comprises a NAND gate

26. The integrated circuit of claim 15, wherein the p-channel transistor serves as a pull-up transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in said CMOS circuit.

27. The integrated circuit of claim 15, wherein the CMOS circuit comprises an inverter

28. A method of fabricating a CMOS inverter comprising:

providing a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer; and

integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

29. The method of claim 28, wherein the heterostructure further comprises a planarized surface positioned between the strained surface layer and the Si substrate

30. The method of claim 28, wherein the surface roughness of the strained surface layer is less than 1nm

31. The method of claim 28, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

32. The method of claim 28, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate

33. The method of claim 28, wherein the strained surface layer comprises Si.

34. The method of claim 28, wherein $0.1<x<0.5$

35. The method of claim 34, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in bulk silicon.

36. The method of claim 34, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in the strained surface layer

37. The method of claim 34, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in bulk silicon

38. The method of claim 34, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in the strained surface layer.

39. The method of claim 34, wherein the gate drive is reduced to lower power consumption

40. A method of fabricating an integrated circuit comprising:

providing a heterostructure having a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained layer on said relaxed $Si_{1-x}Ge_x$ layer; and

forming a p transistor and an n transistor in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and said p transistor are interconnected in a CMOS circuit.

41. The method of claim 40, wherein the heterostructure further comprises a planarized surface positioned between the strained layer and the Si substrate

42. The method of claim 40, wherein the surface roughness of the strained layer is less than 1nm

43. The method of claim 40, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate

44. The method of claim 40, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate

45. The method of claim 40, wherein the strained layer comprises Si

46. The method of claim 40, wherein $0.1<x<0.5$

47. The method of claim 40, wherein the CMOS circuit comprises a logic gate

48. The method of claim 40, wherein the CMOS circuit comprises a NOR gate

49. The method of claim 40, wherein the CMOS circuit comprises an XOR gate

50. The method of claim 40, wherein the CMOS circuit comprises a NAND gate

51. The method of claim 40, wherein the p-channel transistor serves as a pull-up transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in said CMOS circuit

52. The method of claim 40, wherein the CMOS circuit comprises an inverter

53. A method of fabricating a CMOS inverter comprising:
providing a graded $Si_{1-x}Ge_x$ layer on a first Si substrate;
providing a relaxed $Si_{1-y}Ge_y$ layer on said graded layer to form a first structure;
bonding said relaxed layer of said first structure to a second structure that includes a second Si substrate;
removing said first Si substrate and said graded layer;
providing a strained surface layer on said relaxed layer to form a heterostructure; and
integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

54. A method of fabricating an integrated circuit comprising:
providing a graded $Si_{1-x}Ge_x$ layer on a first Si substrate;
providing a relaxed $Si_{1-y}Ge_y$ layer on said graded layer to form a first structure;
bonding said relaxed layer of said first structure to a second structure that includes a second Si substrate;
removing said first Si substrate and said graded layer;
providing a strained surface layer on said relaxed layer to form a heterostructure; and

forming a p transistor and an n transistor in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and said p transistor are interconnected in a CMOS circuit.

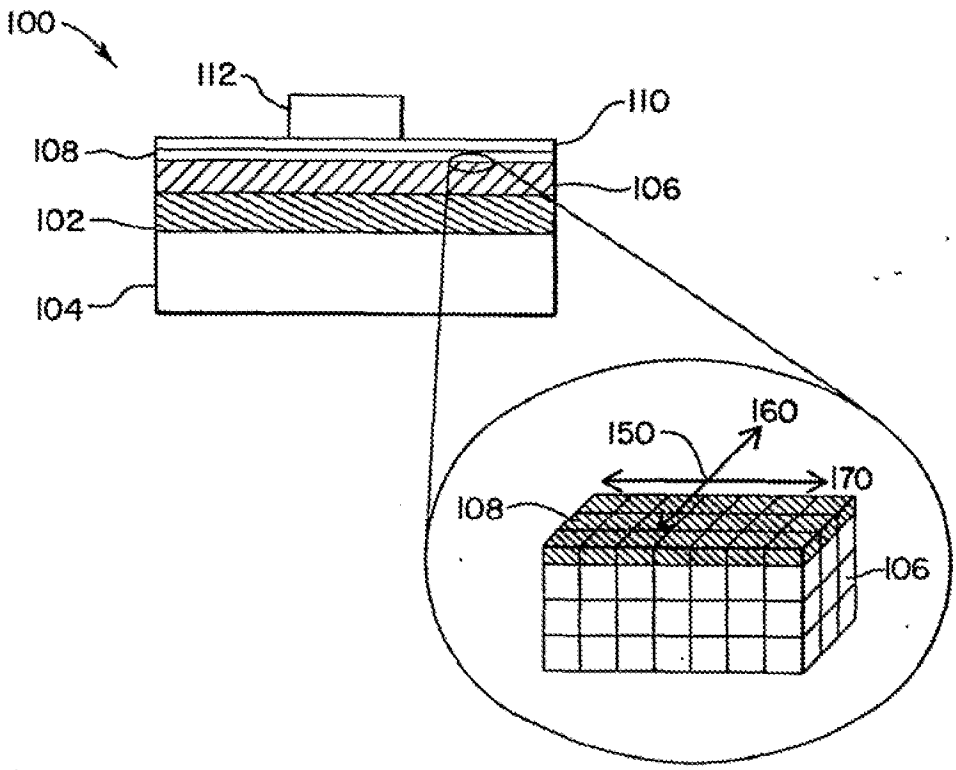

FIG. 1

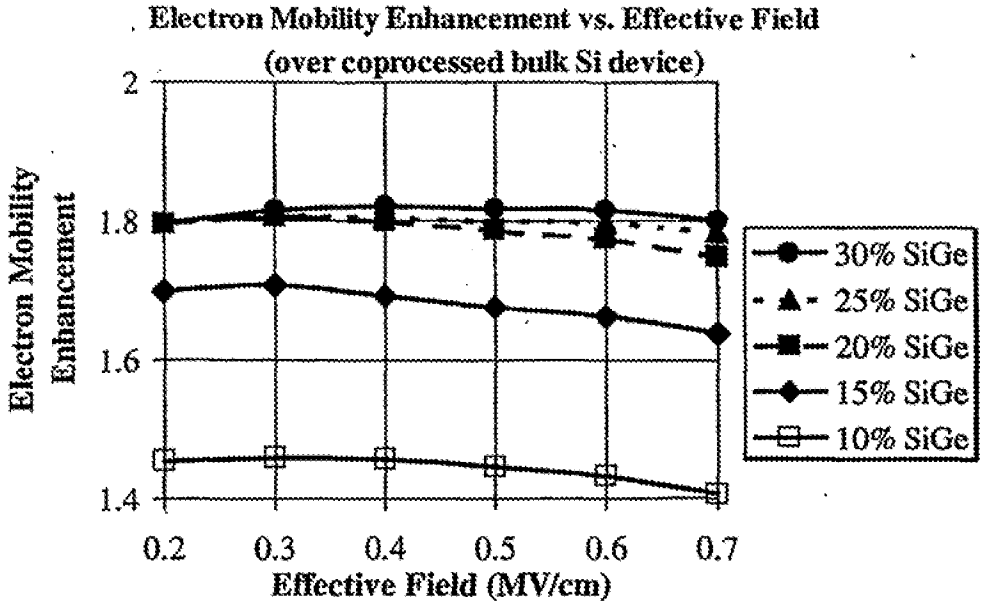

FIG. 2A

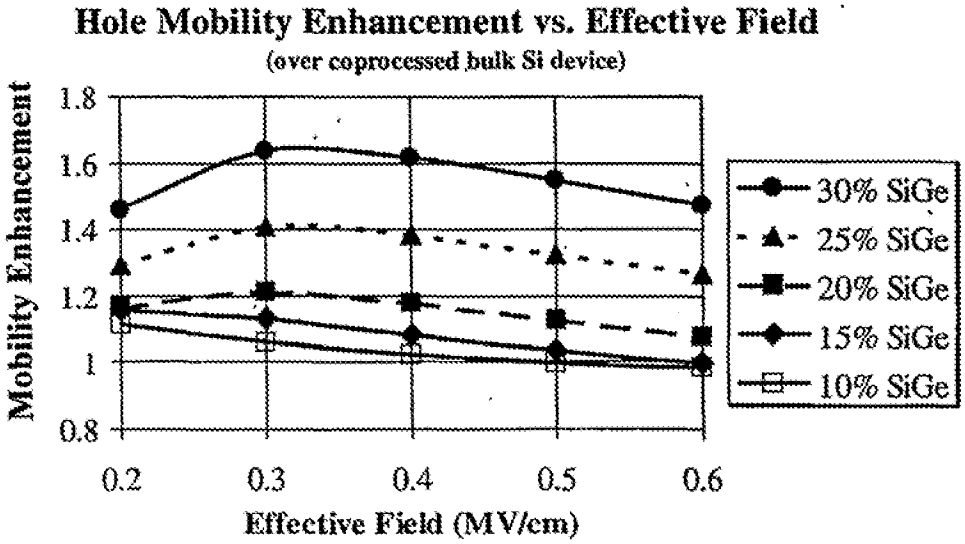

FIG. 2B

Type of Surface	Average Roughness (nm)
As-grown graded composition relaxed SiGe	7.9
Planarized SiGe	0.57
Regrowth SiGe	~0.6

FIG. 3

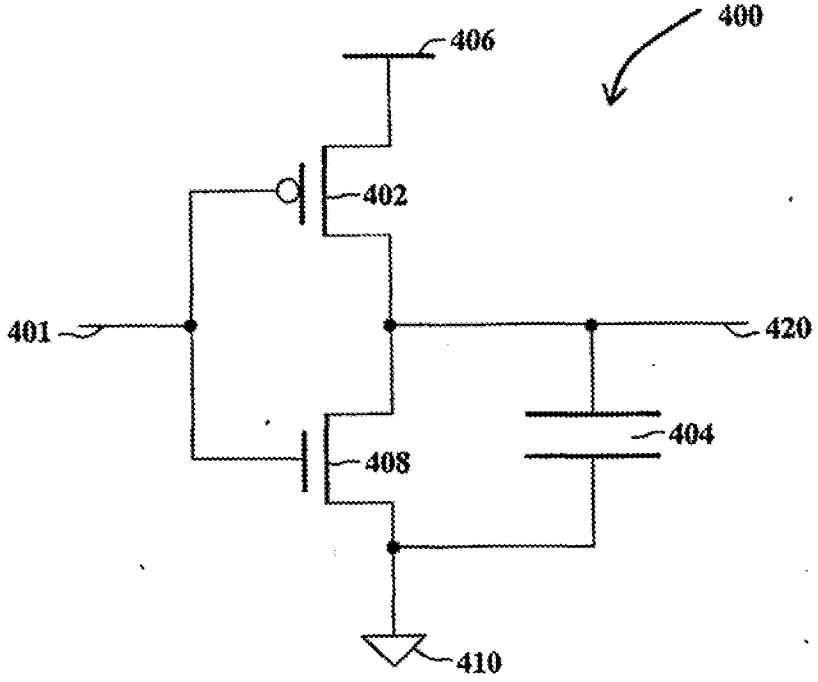
400
406
402
401
420
404
408
410

FIG. 4A

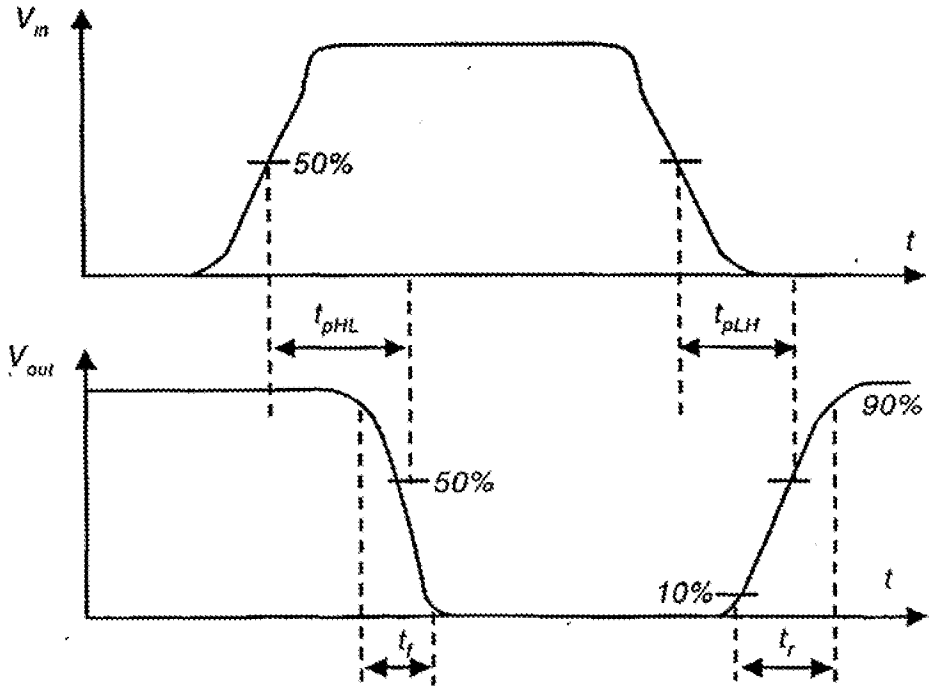
V_{in}
50%
t
t_{pHL}
t_{pLH}
V_{out}
90%
50%
10%
t
t_f
t_r

FIG. 4B

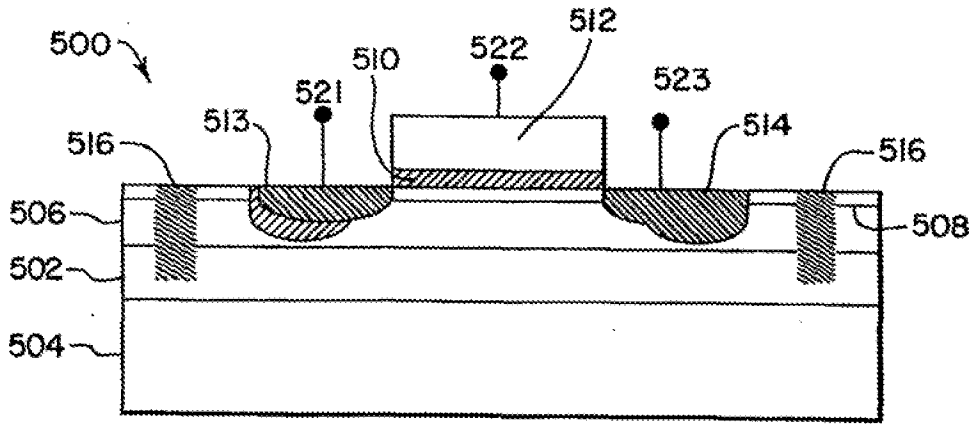

FIG. 5A

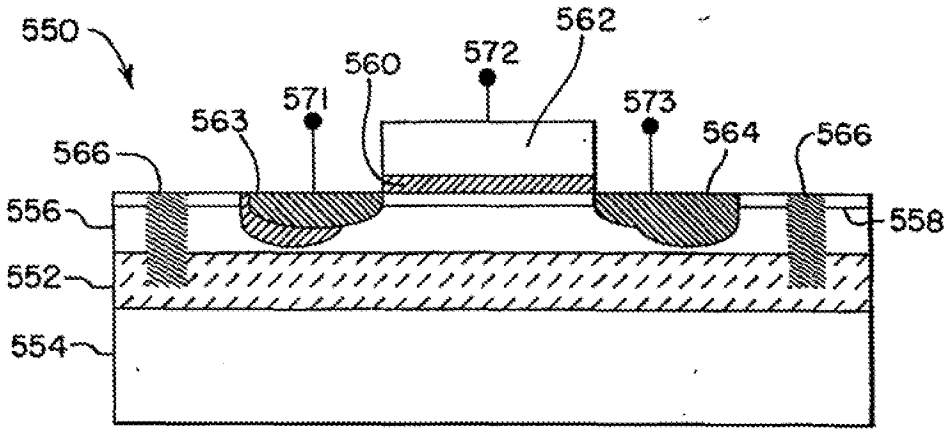

FIG. 5B

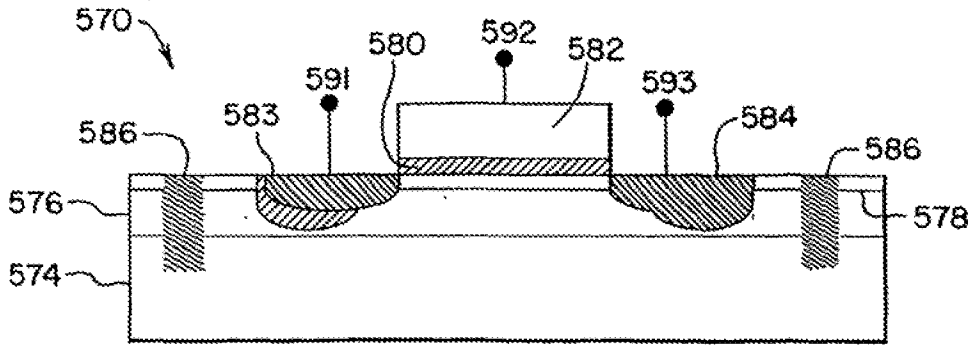

FIG. 5C

	n enhancement	p enhancement
$Si_{0.8}Ge_{0.2}$	1.75	1
$Si_{0.7}Ge_{0.3}$	1.8	1.4

FIG. 6

	Bulk Silicon	Strained-Si on 20% SiGe: High Speed	Strained-Si on 30% SiGe: High Speed	Strained-Si on 20% SiGe: Low Power	Strained-Si on 30% SiGe: Low Power
n enhancement	1	1.75	1.8	1.75	1.8
p enhancement	1	1	1.4	1	1.4
W_p (μm)	5.4	5.4	5.4	5.4	5.4
W_n (μm)	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2
C_L (fF)	32	32	32	32	32
V_{DD} (V)	5	4.7	4.4	4.3	3.8
NM_H (V)	2.053	2.218	1.949	2.037	1.682
NM_L (V)	2.067	1.654	1.721	1.542	1.504
t_{pHL} (psec)	211.3	133.7	141.6	152.2	180.1
t_{pLH} (psec)	195.8	220.0	173.3	254.8	226.9
t_p (psec)	203.5	176.9	157.4	203.5	203.5
Power (mW)	3.93	3.93	3.93	2.87	2.21
% Speed Increase	-	**15.1%**	**29.3%**	-	-
% Power Reduction	-	-	-	**27.0%**	**43.7%**

FIG. 7

	Bulk Silicon	Strained-Si on 20% SiGe: Constant V_{DD}	Strained-Si on 30% SiGe: Constant V_{DD}	Strained-Si on 20% SiGe: High Speed Symmetrical Inverter	Strained-Si on 30% SiGe: High Speed Symmetrical Inverter	Strained-Si on 20% SiGe: Low Power Symmetrical Inverter	Strained-Si on 30% SiGe: Low Power Symmetrical Inverter
n enhancement	1	1.75	1.8	1.75	1.8	1.75	1.8
p enhancement	1	1	1.4	1	1.4	1	1.4
W_p (μm)	5.4	5.4	5.4	9.45	6.94	9.45	6.94
W_n (μm)	1.8	1.8	1.8	1.8	1.8	1.8	1.8
L_m, L_D (μm)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
C_L (fF)	150	150	150	167	156	167	156
V_{DD} (V)	5	5	5	4.28	4.25	3.75	3.55
NM_H (V)	2.05	2.37	2.2	1.78	1.770	1.59	1.51
NM_L (V)	2.07	1.75	1.92	1.79	1.781	1.59	1.52
t_{pHL} (psec)	990	566	550	791	729	967	960
t_{pLH} (psec)	918	918	656	757	697	948	950
t_p (psec)	954	741	603	774	713	957	954
Power (mW)	3.93	5.05	6.22	3.95	3.96	2.45	2.06
% Speed Increase	-	**22.3%**	**36.7%**	**23.0%**	**33.8%**	-	-
% Power Reduction	-	**-28.0%**	**-58.2%**	-	-	**37.6%**	**47.0%**

FIG. 8

	Bulk Silicon	Strained-Si on 20% SiGe: High Speed	Strained-Si on 30% SiGe: High Speed	Strained-Si on 20% SiGe: Low Power	Strained-Si on 30% SiGe: Low Power
n enhancement	1	1.75	1.8	1.75	1.8
p enhancement	1	1	1.4	1	1.4
W_p (μm)	3.11	4.12	3.53	4.12	3.53
W_n (μm)	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2
C_L (fF)	22.5	26.7	24.2	26.7	24.2
V_{DD} (V)	5	4.5	4.3	4.4	3.8
NM_H (V)	2.370	2.275	2.123	2.220	1.872
NM_L (V)	1.756	1.485	1.511	1.458	1.371
t_{pHL} (psec)	148.4	117.3	109.3	121.5	132.4
t_{pLH} (psec)	238.5	254.8	204.9	265.3	254.4
t_p (psec)	193.4	186.0	157.1	193.4	193.4
Power (mW)	2.90	2.90	2.90	2.66	1.83
% Speed Increase	-	**4.0%**	**23.1%**	-	-
% Power Reduction	-	-	-	**8.4%**	**37.1%**

FIG. 9

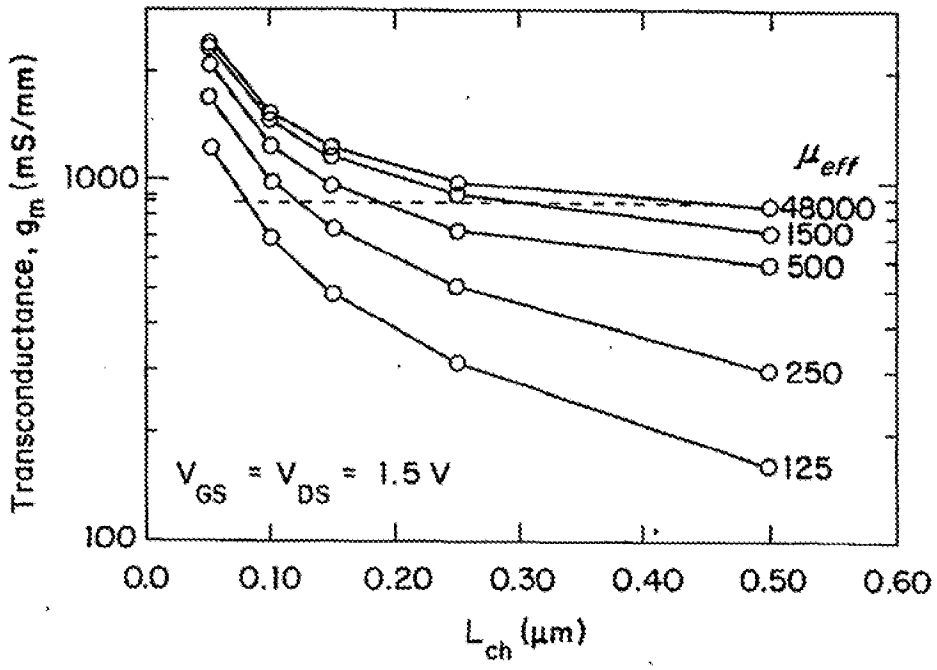
Transconductance, g_m (mS/mm)
1000
100
0.0
0.10
0.20
0.30
0.40
0.50
0.60
L_{ch} (μm)
μ_{eff}
48000
1500
500
250
125
$V_{GS} = V_{DS} = 1.5$ V

FIG. 10

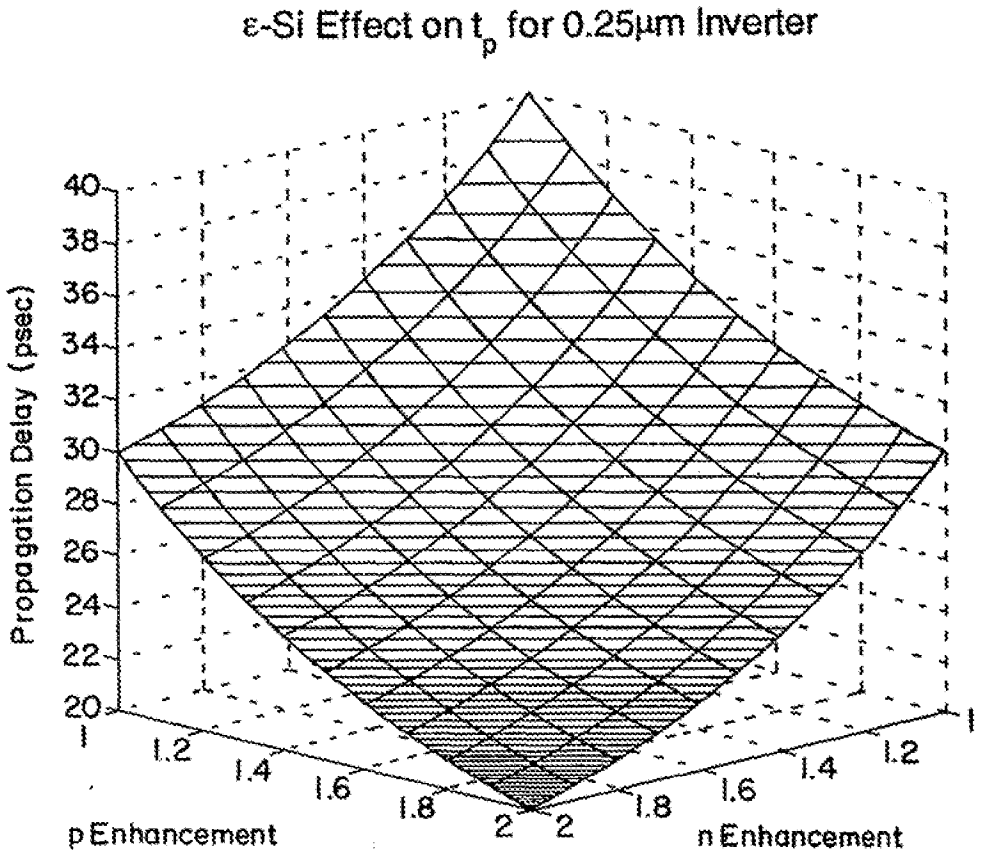
ε-Si Effect on t_p for 0.25μm Inverter
Propagation Delay (psec)
40
38
36
34
32
30
28
26
24
22
20
1
1.2
1.4
1.6
1.8
2
p Enhancement
2
1.8
1.6
1.4
1.2
1
n Enhancement

FIG. 11

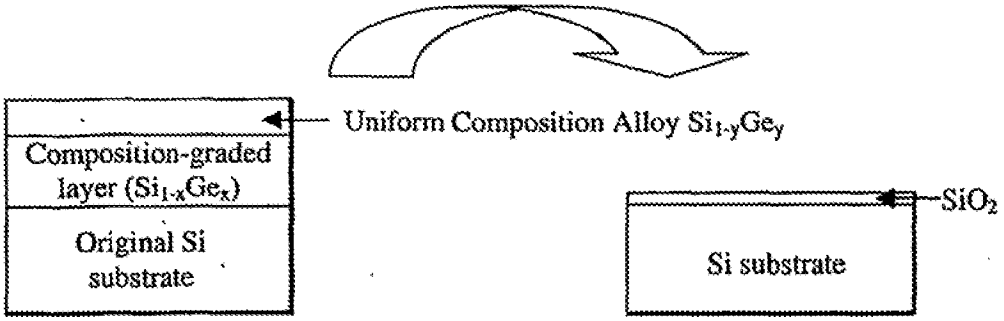

FIG. 12A FIG. 12B

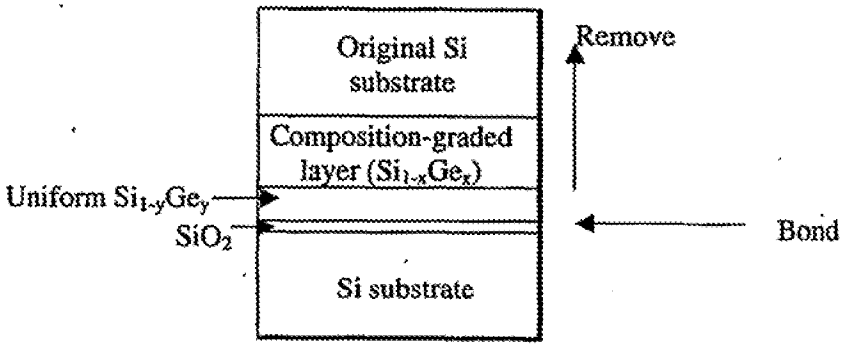

FIG. 12C

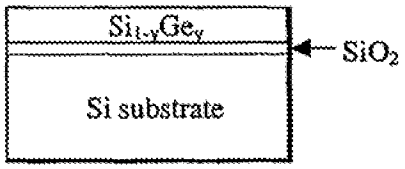

FIG. 12D

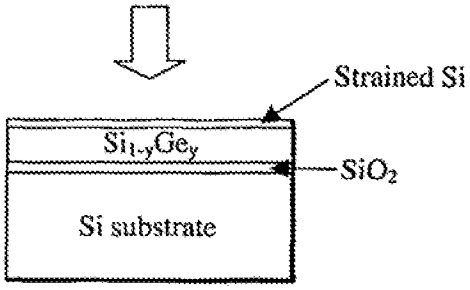

FIG. 12E

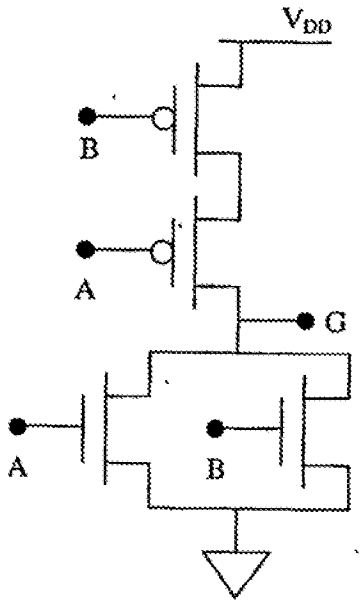

FIG. 13A

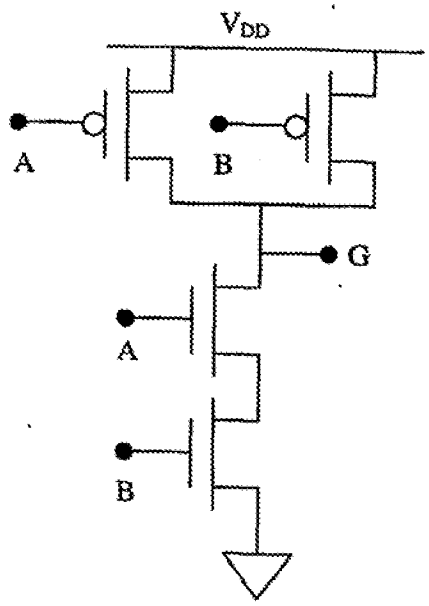

FIG. 13B

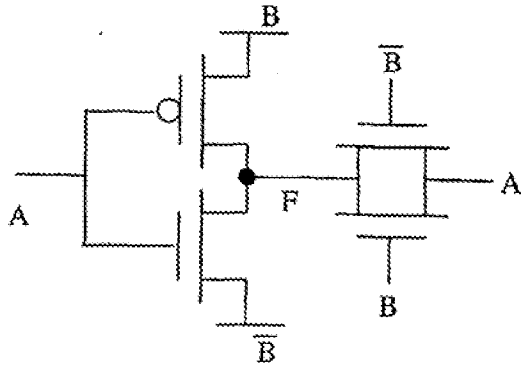

FIG. 13C

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09/906,533	16 July 2001 (16.07.2001)	US

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(72) Inventor: FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US).

(74) Agents: CONNORS, Matthew, E. et al.; Samuels, Gauthier & Stevens, LLP, Suite 3300, 225 Franklin Street, Boston, MA 02110 (US).

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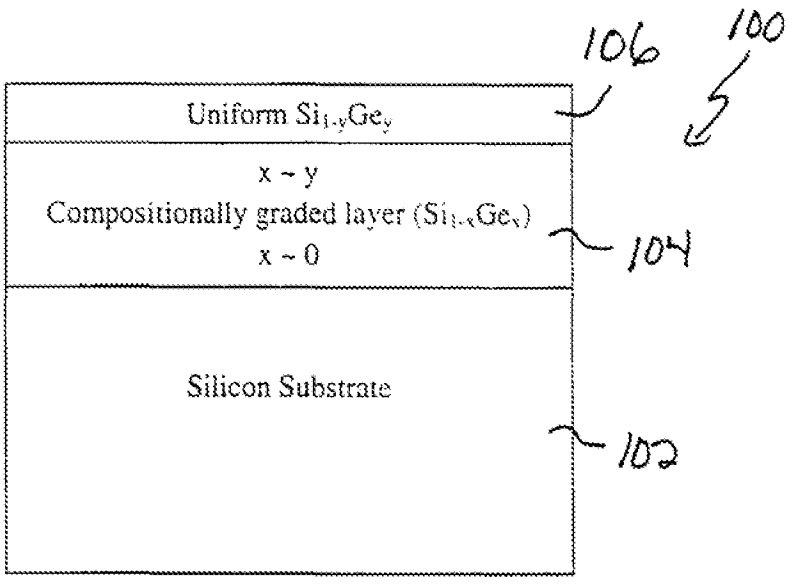
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: RELAXED SILICON GERMANIUM PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS



(57) Abstract: Structures and methods for fabricating high speed digital, analog, and combined digital/analog systems using planarized relaxed SiGe as the materials platform. The relaxed SiGe allows for a plethora of strained Si layers that possess enhanced electronic properties. By allowing the MOSFET channel to be either at the surface or buried, one can create high-speed digital and/or analog circuits. The planarization before the device epitaxial layers are deposited ensures a flat surface for state-of-the-art lithography.

WO 02/071488 A1

RELAXED SILICON GERMANIUM PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS

PRIORITY INFORMATION

This application claims priority from U.S. Patent Applications Nos. 09/906,438 and 09/906,533 both filed on July 16, 2001, which claim priority to U.S. provisional application Ser. No. 60/273,112 filed March 2, 2001.

BACKGROUND OF THE INVENTION

The invention relates to the field of relaxed SiGe platforms for high speed CMOS electronics and high speed analog circuits.

Si CMOS as a platform for digital integrated circuits has progressed predictably through the industry roadmap. The progress is created through device miniaturization, leading to higher performance, greater reliability, and lower cost. However, new bottlenecks in data flow are appearing as the interconnection hierarchy is expanded. Although digital integrated circuits have progressed at unprecedented rates, analog circuitry has hardly progressed at all. Furthermore, it appears that in the near future, serious economic and technological issues will confront the progress of digital integrated circuits.

The digital and communication chip markets need an enhancement to Si CMOS and the maturing roadmap. One promising candidate material that improves digital integrated circuit technology and introduces new analog integrated circuit possibilities is relaxed SiGe material on Si substrates. Relaxed SiGe alloys on Si can have thin layers of Si deposited on them, creating tension in the thin Si layers. Tensile Si layers have many advantageous properties for the basic device in integrated circuits, the metal-oxide field effect transistor (MOSFET). First, placing Si in tension increases the mobility of electrons moving parallel to the surface of the wafer, thus increasing the frequency of operation of the MOSFET and the associated circuit. Second, the band offset between the relaxed SiGe and the tensile Si will confine electrons in the Si layer. Therefore, in an electron channel device (n-channel), the channel can be removed from the surface or 'buried'. This ability to spatially separate the charge carriers from scattering centers such as ionized impurities and the 'rough' oxide interface enables the production of low noise, high performance analog devices and circuits.

A key development in this field was the invention of relaxed SiGe buffers with low

threading dislocation densities. The key background inventions in this area are described in U.S. Pat. No. 5,442,205 issued to Brasen et al. and U.S. Pat. No. 6,107,653 issued to Fitzgerald. These patents define the current best methods of fabricating high quality relaxed SiGe.

Novel device structures in research laboratories have been fabricated on early, primitive versions of the relaxed buffer. For example, strained Si, surface channel nMOSFETs have been created that show enhancements of over 60% in intrinsic g_m with electron mobility increases of over 75% (Rim et al, IEDM 98 Tech. Dig. p. 707). Strained Si, buried channel devices demonstrating high transconductance and high mobility have also been fabricated (U. Konig, MRS Symposium Proceedings 533, 3 (1998)). Unfortunately, these devices possess a variety of problems with respect to commercialization. First, the material quality that is generally available is insufficient for practical utilization, since the surface of SiGe on Si becomes very rough as the material is relaxed via dislocation introduction. These dislocations are essential in the growth of relaxed SiGe layers on Si since they compensate for the stress induced by the lattice mismatch between the materials. For more than 10 years, researchers have tried to intrinsically control the surface morphology through epitaxial growth, but since the stress fields from the misfit dislocations affect the growth front, no intrinsic epitaxial solution is possible. The invention describes a method of planarization and regrowth that allows all devices on relaxed SiGe to possess a significantly flatter surface. This reduction in surface roughness increases the yield for fine-line lithography, thus enabling the manufacture of strained Si devices.

A second problem with the strained Si devices made to date is that researchers have been concentrating on devices optimized for very different applications. The surface channel devices have been explored to enhance conventional MOSFET devices, whereas the buried channel devices have been constructed in ways that mimic the buried channel devices previously available only in III-V materials systems, like AlGaAs/GaAs. Recognizing that the Si manufacturing infrastructure needs a materials platform that is compatible with Si, scalable, and capable of being used in the plethora of Si integrated circuit applications, the disclosed invention provides a platform that allows both the enhancement of circuits based on Si CMOS, as well as the fabrication of analog circuits. Thus, high performance analog or digital systems can be designed with this platform. An additional advantage is that both types of circuits can be fabricated in the CMOS process, and therefore a combined, integrated digital/analog system can be designed as a single-chip solution.

With these advanced SiGe material platforms, it is now possible to provide a variety of device and circuit topologies that take advantage of this new materials system. Exemplary embodiments of the invention describe structures and methods to fabricate advanced strained-layer Si devices, and structures and methods to create circuits based on a multiplicity of devices, all fabricated from the same starting material platform. Starting from the same material platform is key to minimizing cost as well as to allowing as many circuit topologies to be built on this platform as possible.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a material platform of planarized relaxed SiGe with regrown device layers. The planarization and regrowth strategy allows device layers to have minimal surface roughness as compared to strategies in which device layers are grown without planarization. This planarized and regrown platform is a host for strained Si devices that can possess optimal characteristics for both digital and analog circuits. Structures and processes are described that allow for the fabrication of high performance digital logic or analog circuits, but the same structure can be used to host a combination of digital and analog circuits, forming a single system-on-chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a structure including a relaxed SiGe layer epitaxially grown on a Si substrate;

FIG. 2 is a schematic block diagram of an exemplary structure showing that the origin of the crosshatch pattern is the stress fields from injected misfit dislocations;

FIG. 3 is a table showing surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates;

FIGs. 4A–4D show an exemplary process flow and resulting platform structure in accordance with the invention;

FIGs. 5A-5D are schematic diagrams of the corresponding process flow and layer structure for a surface channel FET platform in accordance with the invention;

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure for a buried channel FET platform in accordance with the invention;

FIGs. 7A-7D are schematic diagrams of a process flow for a surface channel MOSFET in accordance with the invention;

FIGs. 8A and 8B are schematic block diagrams of surface channel devices with

protective layers;

FIGs. 9A and 9B are schematic block diagrams of surface channel devices with Si layers on Ge-rich layers for use in silicide formation;

FIGs. 10 is schematic diagram of a buried channel MOSFET after device isolation in accordance with the invention;

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention;

FIGs. 12A-12D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the top strained Si layer in accordance with the invention;

FIGs. 13A-13D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the buried strained Si layer in accordance with the invention; and

FIGs. 14A and 14B are schematic diagrams of surface and buried channel devices with $Si_{1-y}Ge_y$ channels on a relaxed $Si_{1-z}Ge_z$ layer.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic block diagram of a structure 100 including a relaxed SiGe layer epitaxially grown on a Si substrate 102. In this structure, a compositionally graded buffer layer 104 is used to accommodate the lattice mismatch between the uniform SiGe layer 106 and the Si substrate. By spreading the lattice mismatch over a distance, the graded buffer minimizes the number of dislocations reaching the surface and thus provides a method for growing high-quality relaxed SiGe films on Si.

Any method of growing a high-quality, relaxed SiGe layer on Si will produce roughness on the surface of the SiGe layer in a well-known crosshatch pattern. This crosshatch pattern is typically a few hundred angstroms thickness over distances of microns. Thus, the crosshatch pattern is a mild, undulating surface morphology with respect to the size of the electron or hole. For that reason, it is possible to create individual devices that achieve enhancements over their control Si device counterparts. However, commercialization of these devices requires injection of the material into the Si CMOS process environment to achieve low cost, high performance targets. This processing environment requires that the material and device characteristics have minimal impact on the manufacturing process. The crosshatch pattern on the surface of the wafer is one limiting characteristic of relaxed SiGe on Si that affects the yield and the ease of manufacture. Greater planarity is desired for high yield and ease in

lithography.

The origin of the crosshatch pattern is the stress fields from the injected misfit dislocations. This effect is depicted by the exemplary structure 200 shown in FIG. 2. By definition, the dislocations must be introduced in order to accommodate the lattice-mismatch between the SiGe alloy and the Si substrate. The stress fields originate at the dislocations, and are terminated at the surface of the film. However, the termination at the surface creates crystal lattices that vary from place to place on the surface of the wafer. Since growth rate can be correlated to lattice constant size, different thicknesses of deposition occur at different points on the wafer. One may think that thick layer growth beyond the misfit dislocations will smooth the layer of these thickness differences. Unfortunately, the undulations on the surface have a relatively long wavelength; therefore, surface diffusion is typically not great enough to remove the morphology.

FIG. 3 is a table that displays surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates. Note that the as-grown crosshatch pattern for relaxed $Si_{0.8}Ge_{0.2}$ buffers creates a typical roughness of approximately 7.9nm. This average roughness increases as the Ge content in the relaxed buffer is increased. Thus, for any SiGe layer that is relaxed through dislocation introduction during growth, the surface roughness is unacceptable for state-of-the-art fabrication facilities. After the process in which the relaxed SiGe is planarized, the average roughness is less than 2nm (typically 0.57nm), and after device layer deposition, the average roughness is 0.77nm with a 1.5μm regrowth thickness. Therefore, after the complete structure is fabricated, over one order of magnitude of roughness reduction can be achieved.

The regrowth device layers can be either greater than or less than the critical thickness of the regrowth layer. In general, in any lattice-mismatched epitaxial growth, thin layers can be deposited without fear of dislocation introduction at the interface. At a great enough thickness, any lattice-mismatch between the film and substrate will introduce misfit dislocations into the regrown heterostructure. These new dislocations can cause additional surface roughness. Thus, if the lattice-mismatch between the regrowth device layers and relaxed SiGe buffer is too great, the effort of planarizing the relaxed SiGe may be lost since massive dislocation introduction will roughen the surface.

There are two distinct possibilities with respect to the regrowth thickness and the quality of surface. If the regrowth layers are very thin, then exact lattice matching

of the regrowth layer composition and the relaxed buffer composition is not necessary. In this case, the surface roughness will be very low, approximately equal to the post-planarization flatness. However, in many applications for devices, the regrowth layer thickness will be 1-2μm or more. For a 1% difference in Ge concentration between the relaxed SiGe and the regrowth layer, the critical thickness is approximately 0.5μm. Thus, if optimal flatness is desired, it is best to keep the regrowth layer below approximately 0.5μm unless excellent control of the uniformity of Ge concentration across the wafer is achieved. Although this composition matching is achievable in state-of-the-art tools, FIG. 3 shows that less precise matching, i.e., within 2% Ge, results in misfit dislocation introduction and introduction of a new crosshatch pattern. However, because the lattice mismatch is so small, the average roughness is still very low, approximately 0.77nm. Thus, either lattice-matching or slight mismatch will result in excellent device layer surfaces for processing.

It is also noted that the relaxed SiGe alloy with surface roughness may not necessarily be a uniform composition relaxed SiGe layer on a graded composition layer. Although this material layer structure has been shown to be an early example of high quality relaxed SiGe, there are some disadvantages to this structure. For example, SiGe alloys possess a much worse coefficient of thermal conductivity than pure Si. Thus, for electronic devices located at the surface, it may be relatively difficult to guide the heat away from the device areas due to the thick graded composition layer and uniform composition layer.

Another exemplary embodiment of the invention, shown in FIGs. 4A-4D, solves this problem and creates a platform for high power SiGe devices. FIGs. 4A--4D show an exemplary process flow and resulting platform structure in accordance with the invention. The structure is produced by first forming a relaxed uniform SiGe alloy 400 via a compositionally graded layer 402 on a Si substrate 404. The SiGe layer 400 is then transferred to a second Si substrate 406 using conventional bonding. For example, the uniform SiGe alloy 400 on the graded layer 402 can be planarized to remove the crosshatch pattern, and that relaxed SiGe alloy can be bonded to the Si wafer. The graded layer 402 and the original substrate 404 can be removed by a variety of conventional processes. For example, one process is to grind the original Si substrate away and selectively etch to the SiGe, either by a controlled dry or wet etch, or by embedding an etch stop layer. The end result is a relaxed SiGe alloy 400 on Si without the thick graded layer. This structure is more suited for high power applications since the heat can be conducted away from the SiGe layer more efficiently. The bond and substrate removal

technique can also be used to produce SiGe on insulator substrates, or SGOI. An SGOI wafer is produced using the same technique shown in FIGs. 4A-4D; however, the second substrate is coated with a SiO_2 layer before bonding. In an alternative embodiment, both wafers can be coated with SiO_2 to enable oxide-to-oxide bonding. The resulting structure after substrate removal is a high quality, relaxed SiGe layer on an insulating film. Devices built on this platform can utilize the performance enhancements of both strained Si and the SOI architecture.

It will be appreciated that in the scenario where the SiGe layer is transferred to another host substrate, one may still need to planarize before regrowing the device layer structure. The SiGe surface can be too rough for state of the art processing due to the substrate removal technique. In this case, the relaxed SiGe is planarized, and the device layers are regrown on top of the high-quality relaxed SiGe surface.

Planarization of the surface via mechanical or other physical methods is required to flatten the surface and to achieve CMOS-quality devices. However, the field effect transistors (FETs) that allow for enhanced digital and analog circuits are very thin, and thus would be removed by the planarization step. Thus, a first part of the invention is to realize that relaxed SiGe growth and planarization, followed by device layer regrowth, is key to creating a high-performance, high yield enhanced CMOS platform. FIGs. 5 and 6 show the process sequence and regrowth layers required to create embodiments of surface channel and buried channel FETs, respectively.

FIGs. 5A-5D are schematic diagrams of a process flow and resulting layer structure in accordance with the invention. FIG. 5A shows the surface roughness 500, which is typical of a relaxed SiGe alloy 502 on a substrate 504, as an exaggerated wavy surface. Note that the substrate is labeled in a generic way, since the substrate could itself be Si, a relaxed compositionally graded SiGe layer on Si, or another material in which the relaxed SiGe has been transferred through a wafer bonding and removal technique. The relaxed SiGe alloy 502 is planarized (FIG. 5B) to remove the substantial roughness, and then device regrowth layers 506 are epitaxially deposited (FIG. 5C). It is desirable to lattice-match the composition of the regrowth layer 506 as closely as possible to the relaxed SiGe 502; however, a small amount of mismatch and dislocation introduction at the interface is tolerable since the surface remains substantially planar. For a surface channel device, a strained Si layer 508 of thickness less than 0.1μm is then grown on top of the relaxed SiGe 502 with an optional sacrificial layer 510, as shown in FIG. 5D. The strained layer 508 is the layer that will be used as the channel in the final CMOS devices.

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure for a buried channel FET platform in accordance with the invention. In this structure, the regrowth layers 606 include a lattice matched SiGe layer 602, a strained Si channel layer 608 with a thickness of less than 0.05μm, a SiGe separation or spacer layer 612, a Si gate oxidation layer 614, and an optional sacrificial layer 610 used to protect the heterostructure during the initial device processing steps.

Once the device structure has been deposited, the rest of the process flow for device fabrication is very similar to that of bulk Si. A simplified version of the process flow for a surface channel MOSFET in accordance with the invention is shown in FIGs. 7A-7D. This surface channel MOSFET contains a relaxed SiGe layer 700 and a strained Si layer 702. The device isolation oxide 704, depicted in FIG. 7A, is typically formed first. In this step, the SiN layer 706, which is on top of a thin pad oxide layer 708, serves as a hard mask for either local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Both techniques use a thick oxide (relative to device dimensions) to provide a high threshold voltage between devices; however, STI is better suited for sub-quarter-micron technologies. Figure 7B is a schematic of the device area after the gate oxide 716 growth and the shallow-source drain implant. The implant regions 710 are self-aligned by using a poly-Si gate 712 patterned with photoresist 714 as a masking layer. Subsequently, deep source-drain implants 718 are positioned using conventional spacer 720 formation and the device is electrically contacted through the formation of silicide 722 at the gate and silicide/germanides 724 at the source and drain (Figure 7C). Figure 7D is a schematic of the device after the first level of metal interconnects 726 have been deposited and etched.

Since there are limited-thickness layers on top of the entire structure, the removal of surface material during processing becomes more critical than with standard Si. For surface channel devices, the structure that is regrown consists primarily of nearly lattice-matched SiGe, and a thin surface layer of strained Si. Many of the processes that are at the beginning of a Si fabrication sequence strip Si from the surface. If the processing is not carefully controlled, the entire strained Si layer can be removed before the gate oxidation. The resulting device will be a relaxed SiGe channel FET and thus the benefits of a strained Si channel will not be realized.

A logical solution to combat Si removal during initial processing is to make the strained Si layer thick enough to compensate for this removal. However, thick Si layers are not possible for two reasons. First, the enhanced electrical properties originate from the fact that the Si is strained and thick layers experience strain relief through the

introduction of misfit dislocations. Second, the misfit dislocations themselves are undesirable in significant quantity, since they can scatter carriers and increase leakage currents in junctions.

In order to prevent removal of strained Si layers at the surface, the cleaning procedures before gate oxidation must be minimized and/or protective layers must be applied. Protective layers are useful since their removal can be carefully controlled. Some examples of protective layers for surface channel devices are shown in FIGS. 8A and 8B. FIG. 8A shows a strained Si heterostructure of a relaxed SiGe layer 800 and a strained Si channel layer 802 protected by a surface layer 804 of SiGe. The surface SiGe layer 804 should have a Ge concentration similar to that of the relaxed SiGe layer 800 below, so that the thickness is not limited by critical thickness constraints. During the initial cleans, the SiGe sacrificial layer is removed instead of the strained Si channel layer. The thickness of the sacrificial layer can either be tuned to equal the removal thickness, or can be made greater than the removal thickness. In the latter case, the excess SiGe can be selectively removed before the gate oxidation step to reveal a clean, strained Si layer at the as grown thickness. If the particular fabrication facility prefers a Si terminated surface, a sacrificial Si layer may be deposited on top of the SiGe sacrificial cap layer.

FIG. 8B shows a structure where a layer 806 of SiO_2 and a surface layer 808 of either a poly-crystalline or an amorphous material are used as protective layers. In this method, an oxide layer is either grown or deposited after the epitaxial growth of the strained Si layer. Subsequently, a polycrystalline or amorphous layer of Si, SiGe, or Ge is deposited. These semiconductor layers protect the strained-Si layer in the same manner as a SiGe cap during the processing steps before gate oxidation. Prior to gate oxidation, the poly/amorphous and oxide layers are selectively removed. Although the sacrificial layers are shown as protection for a surface channel device, the same techniques can be employed in a buried channel heterostructure.

Another way in which conventional Si processing is modified is during the source-drain silicide-germanide formation (FIG. 7C). In conventional Si processing, a metal (typically Ti, Co, or Ni) is reacted with the Si and, through standard annealing sequences, low resistivity silicides are formed. However, in this case, the metal reacts with both Si and Ge simultaneously. Since the silicides have much lower free energy than the germanides, there is a tendency to form a silicide while the Ge is expelled. The expelled germanium creates agglomeration and increases the resistance of the contacts. This increase in series resistance offsets the benefits of the extra drive current

from the heterostructure, and negates the advantages of the structure.

Ti and Ni can form phases in which the Ge is not rejected severely, thus allowing the formation of a good contact. Co is much more problematic. However, as discussed above for the problem of Si removal, a protective layer(s) at the device epitaxy stage can be applied instead of optimizing the SiGe-metal reaction. For example, the strained Si that will become the surface channel can be coated with a high-Ge-content SiGe alloy (higher Ge content than the initial relaxed SiGe), followed by strained Si. Two approaches are possible using these surface contact layers. Both methods introduce thick Si at the surface and allow the conventional silicide technology to be practiced without encountering the problems with SiGe-metal reactions.

The first approach, shown on a surface channel heterostructure 900 in FIG. 9A, uses a Ge-rich layer 906 thin enough that it is substantially strained. The layer 906 is provided on a strained Si channel layer 904 and relaxed SiGe layer 902. In this case, if a subsequent Si layer 908 is beyond the critical thickness, the compressive Ge-rich layer 906 acts as a barrier to dislocations entering the strained Si channel 904. This barrier is beneficial since dislocations do not adversely affect the silicide process; thus, their presence in the subsequent Si layer 908 is of no consequence. However, if the dislocations were to penetrate to the channel, there would be adverse effects on the device.

A second approach, shown in FIG. 9B, is to allow a Ge-rich layer 910 to intentionally exceed the critical thickness, thereby causing substantial relaxation in the Ge-rich layer. In this scenario, an arbitrarily thick Si layer 912 can be applied on top of the relaxed Ge-rich layer. This layer will contain more defects than the strained channel, but the defects play no role in device operation since this Si is relevant only in the silicide reaction. In both cases, the process is free from the metal-SiGe reaction concerns, since the metal will react with Si-only.

Once the silicide contacts have been formed, the rest of the sequence is a standard Si CMOS process flow, except that the thermal budget is carefully monitored since, for example, the silicide-germanicide (if that option is used) typically cannot tolerate as high a temperature as the conventional silicide. A major advantage of using Si/SiGe FET heterostructures to achieve enhanced performance is the compatibility with conventional Si techniques. Many of the processes are identical to Si CMOS processing, and once the front-end of the process, i.e., the processing of the Si/SiGe heterostructure, is complete, the entire back-end process is uninfluenced by the fact that Si/SiGe lies below.

Even though the starting heterostructure for the buried channel device is different from that of the surface channel device, its process flow is very similar to the surface channel flow shown in FIGs. 7A-7D. FIG. 10 is a schematic block diagram of a buried channel MOSFET structure 1000 after the device isolation oxide 1016 has been formed using a SiN mask 1014. In this case, the strained channel 1002 on a first SiGe layer 1010 is separated from the surface by the growth of another SiGe layer 1004, followed by another Si layer 1006. This Si layer is needed for the gate oxide 1008 since gate-oxide formation on SiGe produces a very high interface state density, thus creating non-ideal MOSFETs. One consequence of this Si layer, is that if it is too thick, a substantial portion of the Si layer will remain after the gate oxidation. Carriers can populate this residual Si layer, creating a surface channel in parallel with the desired buried channel and leading to deleterious device properties. Thus, the surface layer Si must be kept as thin as possible, typically less than 50Å and ideally in the range of 5-15Å.

Another added feature that is necessary for a buried channel device is the supply layer implant. The field experienced in the vertical direction when the device is turned on is strong enough to pull carriers from the buried channel 1002 and force them to populate a Si channel 1006 near the Si/SiO_2 interface 1012, thus destroying any advantage of the buried channel. Thus, a supply layer of dopant must be introduced either in the layer 1004 between the buried channel and the top Si layer 1006, or below the buried channel in the underlying SiGe 1010. In this way, the device is forced on with little or no applied voltage, and turned off by applying a voltage (depletion mode device).

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention. The main process steps are shown in the boxes, and optional steps or comments are shown in the circles. The first three steps (1100,1102,1104) describe the fabrication of the strained silicon heterostructure. The sequence includes production of relaxed SiGe on Si, planarization of the SiGe, and regrowth of the device layers. Once the strained heterostructure is complete (1106), MOS fabrication begins with device isolation (1112) using either STI (1110) or LOCOS (1108). Before proceeding to the gate oxidation, buried channel devices undergo a supply and threshold implant (1114), and any protective layers applied to either a buried or surface channel heterostructure must be selectively removed (1116). The processing sequence after the gate oxidation (1118) is similar to conventional Si CMOS processing. These steps include gate deposition, doping, and definition (1120), self-aligned shallow source-drain implant (1122), spacer formation (1124), self-aligned deep source-drain

implant (1126), salicide formation (1128), and pad isolation via metal deposition and etch (1130). The steps requiring significant alteration have been discussed.

One particular advantage of the process of FIG. 11 is that it enables the use of surface channel and buried channel devices on the same platform. Consider FIGs. 12A-12D and FIGs. 13A-13D, which show a universal substrate layer configuration and a process that leads to the co-habitation of surface and buried channel MOSFETs on the same chip. The universal substrate is one in which both surface channel and buried channel devices can be fabricated. There are two possibilities in fabricating the surface channel device in this sequence, shown in FIGs. 12 and 13. The process flows for combining surface and buried channel are similar to the previous process described in FIG. 7. Therefore, only the critical steps involved in exposing the proper gate areas are shown in FIGs. 12 and 13.

FIGs. 12A and 13A depict the same basic heterostructure 1200,1300 for integrating surface channel and buried channel devices. There is a surface strained Si layer 1202,1302, a SiGe spacer layer 1204,1304, a buried strained Si layer 1206,1306, and a relaxed platform of SiGe 1208,1308. Two strained Si layers are necessary because the buried channel MOSFET requires a surface Si layer to form the gate oxide and a buried Si layer to form the device channel. The figures also show a device isolation region 1210 that separates the buried channel device area 1212,1312 from the surface channel device area 1214,1314.

Unlike the buried channel device, a surface channel MOSFET only requires one strained Si layer. As a result, the surface channel MOSFET can be fabricated either in the top strained Si layer, as shown in FIGs. 12B-12D, or the buried Si layer channel, as shown in FIGs. 13B-13D. FIG. 12B is a schematic diagram of a surface channel gate oxidation 1216 in the top Si layer 1202. In this scenario, a thicker top Si layer is desired, since after oxidation, a residual strained Si layer must be present to form the channel. FIG. 12B also shows a possible position for the buried channel supply implant 1218, which is usually implanted before the buried channel gate oxide is grown. Since the top Si layer is optimized for the surface channel device, it may be necessary to strip some of the top strained Si in the regions 1220 where buried channel devices are being created, as shown in FIG. 12C. This removal is necessary in order to minimize the surface Si thickness after gate oxide 1222 formation (FIG. 12D), and thus avoid the formation of a parallel device channel.

When a surface channel MOSFET is formed in the buried strained Si layer, the top strained Si layer can be thin, i.e., designed optimally for the buried channel MOSFET. In

FIG. 13B, the top strained Si and SiGe layers are removed in the region 1312 where the surface channel MOSFETs are formed. Because Si and SiGe have different properties, a range of selective removal techniques can be used, such as wet or dry chemical etching. Selective oxidation can also be used since SiGe oxidizes at much higher rates than Si, especially under wet oxidation conditions. FIG. 13C shows the gate oxidation 1314 of the surface channel device as well as the supply layer implant 1316 for the buried channel device. Finally, FIG. 13D shows the position of the buried channel gate oxide 1318. No thinning of the top Si layer is required prior to the oxidation since the epitaxial thickness is optimized for the buried channel device. Subsequent to these initial steps, the processing for each device proceeds as previously described.

Another key step in the process is the use of a localized implant to create the supply layer needed in the buried channel device. In a MOSFET structure, when the channel is turned on, large vertical fields are present that bring carriers to the surface. The band offset between the Si and SiGe that confines the electrons in the buried strained Si layer is not large enough to prevent carriers from being pulled out of the buried channel. Thus, at first, the buried channel MOSFET would appear useless. However, if enough charge were present in the top SiGe layer, the MOSFET would become a depletion-mode device, i.e. normally on and requiring bias to turn off the channel. In the surface/buried channel device platform, a supply layer implant can be created in the regions where the buried channel will be fabricated, thus easing process integration. If for some reason the supply layer implant is not possible, note that the process shown in FIG. 11 in which the surface channel is created on the buried Si layer is an acceptable process, since the dopant can be introduced into the top SiGe layer during epitaxial growth. The supply layer is then removed from the surface channel MOSFET areas when the top SiGe and strained Si layers are selectively etched away.

In the processes described in FIGs. 10, 12 and 13, it is assumed that the desire is to fabricate a buried channel MOSFET. If the oxide of the buried channel device is removed, one can form a buried channel device with a metal gate (termed a MODFET or HEMT). The advantage of this device is that the transconductance can be much higher since there is a decrease in capacitance due to the missing oxide. However, there are two disadvantages to using this device. First, all thermal processes after gate definition have to be extremely low temperature, otherwise the metal will react with the semiconductor, forming an alloyed gate with a very low, or non-existent, barrier. Related to this issue is the second disadvantage. Due to the low thermal budget, the source and drain formation and contacts are typically done before the gate definition. Inverting these steps prevents the gate from

being self-aligned to the source and drain, thus increasing the series resistance between the gate and the source and drain. Therefore, with a carefully designed buried channel MOSFET, the self-aligned nature can be a great advantage in device performance. Another benefit of the MOSFET structure is that the gate leakage is very low.

The combination of buried n-channel structures with n and p type surface channel MOSFETs has been emphasized heretofore. It is important to also emphasize that in buried n-channel devices as well as in surface channel devices, the channels need not be pure Si. $Si_{1-y}Ge_y$ channels can be used to increase the stability during processing. FIGs. 14A and 14B are schematic diagrams of surface 1400 and buried 1450 channel devices with $Si_{1-y}Ge_y$ channels 1402 on a relaxed $Si_{1-z}Ge_z$ layer 1404. The devices are shown after salicidation and thus contain a poly-Si gate 1410, gate oxide 1408, silicide regions 1412, spacers 1414, and doped regions 1416. In the surface channel device 1400, a thin layer 1406 of Si must be deposited onto the $Si_{1-y}Ge_y$ layer 1402 to form the gate oxide 1408, as previously described for buried channel devices. In the buried $Si_{1-y}Ge_y$ channel device 1450, the device layer sequence is unchanged and consists of a buried strained channel 1402, a SiGe spacer layer 1418, and a surface Si layer 1420 for oxidation.

To maintain tensile strain in the channel of an nMOS device, the lattice constant of the channel layer must be less than that of the relaxed SiGe layer, i.e., y must be less than z. Since n-channel devices are sensitive to alloy scattering, the highest mobilities result when the Ge concentration in the channel is low. In order to have strain on this channel layer at a reasonable critical thickness, the underlying SiGe should have a Ge concentration in the range of 10-50%.

Experimental data indicates that p channels are less sensitive to alloy scattering. Thus, surface MOSFETs with alloy channels are also possible. In addition, the buried channel devices can be p-channel devices simply by having the Ge concentration in the channel, y, greater than the Ge concentration in the relaxed SiGe alloy, z, and by switching the supply dopant from n-type to p-type. This configuration can be used to form Ge channel devices when $y = 1$ and $0.5 < z < 0.9$.

With the ability to mix enhancement mode surface channel devices (n and p channel, through implants as in typical Si CMOS technology) and depletion-mode buried channel MOSFETs and MODFETs, it is possible to create highly integrated digital/analog systems. The enhancement mode devices can be fabricated into high performance CMOS, and the regions of an analog circuit requiring the high performance low-noise depletion mode device can be fabricated in the buried channel regions. Thus, it is possible to

construct optimal communication stages, digital processing stages, etc. on a single platform. These different regions are connected electrically in the backend of the Si CMOS chip, just as transistors are connected by the back-end technology today. Thus, the only changes to the CMOS process are some parameters in the processes in the fabrication facility, and the new material, but otherwise, the entire manufacturing process is transparent to the change. Thus, the economics favor such a platform for integrated Si CMOS systems on chip.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A semiconductor structure for integrating surface channel and buried channel devices comprising:

a substrate;

a relaxed $Si_{1-x}Ge_x$ layer;

a $Si_{1-y}Ge_y$ layer;

a $Si_{1-w}Ge_w$ layer; and

a Si layer.

2. The structure of claim 1, wherein a carrier channel of a surface channel device is provided in either said Si layer or said $Si_{1-y}Ge_y$ layer.

3. The structure of claim 1, wherein the semiconductor structure is undoped.

4. The structure of claim 1, wherein $y<x$.

5. The structure of claim 2 or 4, wherein y is approximately 0.

6. The structure of claim 1 further comprising at least one planarized surface.

7. The structure of claim 1, wherein the substrate comprises Si.

8. The structure of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

9. The structure of claim 1, wherein the substrate comprises a graded composition SiGe layer on Si.

10. The structure of claim 9, wherein the substrate further comprises a uniform composition $Si_{1-z}Ge_z$ layer on said graded composition layer.

11. The structure of claim 10, wherein z is approximately equal to x.

12. The structure of claim 11, wherein the surface of the substrate is planarized.

13. The structure of claim 1, wherein the substrate comprises a uniform $Si_{1-z}Ge_z$ layer on Si.

14. The structure of claim 13, wherein z is approximately equal to x.

15. The structure of claim 14, wherein the surface of the substrate is planarized.

16. The structure of claim 13, wherein the $Si_{1-z}Ge_z$ /Si structure is formed through wafer bonding.

17. The structure of claim 13 further comprising a SiO_2 layer between the uniform $Si_{1-z}Ge_z$ layer and the Si.

18. The structure of claim 17, wherein z is approximately equal to x.

19. The structure of claim 18, wherein the surface of the substrate is planarized.

20. A semiconductor structure for integrating surface channel and buried channel devices comprising a relaxed planarized $Si_{1-x}Ge_x$ layer and regrown device layers.

21. The structure of claim 20, wherein the regrown device layers include a $Si_{1-y}Ge_y$ layer of thickness h; a $Si_{1-w}Ge_w$ layer; a $Si_{1-x}Ge_x$ layer having supply dopants; and a Si layer.

22. The structure of claim 21, wherein h is approximately 0.

23. The structure of claim 21, wherein w<x and the supply dopants are n-type.

24. The structure of claim 20, wherein a carrier channel of a surface channel device is provided in either said Si layer or said $Si_{1-w}Ge_w$ layer.

25. An integrated circuit fabricated on relaxed $Si_{1-x}Ge_x$ comprising at least one surface channel MOSFET and at least one buried channel FET.

26. The circuit of claim 25, wherein the surface channel MOSFET comprises a $Si_{1-y}Ge_y$ layer with y<x; a Si layer of thickness h; a gate dielectric; and a highly conductive gate layer.

27. The circuit of claim 26, wherein h and y are approximately 0.

28. The circuit of claim 27, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y<x; a $Si_{1-w}Ge_w$ layer; a Si layer; a gate dielectric; and a highly conductive gate layer.

29. The circuit of claim 28, wherein y is approximately 0.

30. The circuit of claim 27, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y<x; a $Si_{1-w}Ge_w$ layer; a Si layer; and a highly conductive gate layer.

31. The circuit of claim 30, wherein y is approximately 0.

32. The circuit of claim 25, wherein the surface channel MOSFET comprises a $Si_{1-y}Ge_y$ layer with y>x, a $Si_{1-w}Ge_w$ layer; a Si layer; a gate dielectric; and a highly conductive gate layer.

33. The circuit of claim 32, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y>x; a $Si_{1-w}Ge_w$ layer; a Si layer; a gate dielectric; and a highly conductive gate layer.

34. The circuit of claim 33, wherein y is approximately 1.

35. The circuit of claim 32, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y>x; a $Si_{1-w}Ge_w$ layer; a surface Si layer; a highly conductive gate layer.

36. The circuit of claim 35, wherein y is approximately 1.

37. The circuit of claim 25, wherein the relaxed $Si_{1-x}Ge_x$ further comprises at least one planarized surface.

38. A method of fabricating a semiconductor structure comprising:
providing a relaxed $Si_{1-x}Ge_x$ layer on a substrate;
providing a $Si_{1-y}Ge_y$ layer on said $Si_{1-x}Ge_x$ layer;
providing a $Si_{1-w}Ge_w$ layer on said $Si_{1-y}Ge_y$ layer;
providing a Si layer on said $Si_{1-w}Ge_w$ layer, wherein
surface channel and buried channel devices are integrated on said semiconductor structure.

39. The method of claim 38, wherein a carrier channel of a surface channel device is provided in either said Si layer or said $Si_{1-y}Ge_y$ layer.

40. The method of claim 38, wherein the semiconductor structure is undoped.

41. The method of claim 38, wherein y<x.

42. The method of claims 39 or 41, wherein y is approximately 0.

43. The method of claim 38 further comprising planarizing at least one surface.

44. The method of claim 38, wherein the substrate comprises Si.

45. The method of claim 38, wherein the substrate comprises Si with a layer of SiO_2.

46. The method of claim 38, wherein the substrate comprises a graded composition SiGe layer on Si.

47. The method of claim 46, wherein the substrate further comprises a uniform composition $Si_{1-z}Ge_z$ layer on said graded composition layer.

48. The method of claim 47, wherein z is approximately equal to x.

49. The method of claim 48, wherein the surface of the substrate is planarized.

50. The method of claim 38, wherein the substrate comprises a uniform $Si_{1-z}Ge_z$ layer on Si.

51. The method of claim 50, wherein z is approximately equal to x.

52. The method of claim 51, wherein the surface of the substrate is planarized.

53. The method of claim 50, wherein the $Si_{1-z}Ge_z$ /Si structure is formed through wafer bonding.

54. The method of claim 50 further comprising a SiO_2 layer between the uniform $Si_{1-z}Ge_z$ layer and the Si.

55. The method of claim 54, wherein z is approximately equal to x.

56. The method of claim 55, wherein the surface of the substrate is planarized.

57. A method of fabricating a semiconductor structure comprising:

providing a relaxed $Si_{1-x}Ge_x$ layer;

planarizing said relaxed $Si_{1-x}Ge_x$ layer; and

providing regrown device layers on said planarized relaxed $Si_{1-x}Ge_x$ layer, wherein

surface channel and buried channel devices are integrated on said

semiconductor structure.

58. The method of claim 57, wherein the regrown device layers include a $Si_{1-y}Ge_y$ layer of thickness h; a $Si_{1-w}Ge_w$ layer; a $Si_{1-u}Ge_u$ layer having supply dopants; and a Si layer.

59. The method of claim 58, wherein h is approximately 0.

60. The method of claim 58, wherein w<x and the supply dopants are n-type.

61. The method of claim 57, wherein a carrier channel of a surface channel device is provided in either said Si layer or said $Si_{1-w}Ge_w$ layer.

62. A method of fabricating an integrated circuit comprising:

integrating at least one surface channel MOSFET and at least one buried channel FET on a relaxed $Si_{1-x}Ge_x$ layer that is provided on a substrate.

63. The method of claim 62, wherein the surface channel MOSFET comprises a $Si_{1-y}Ge_y$ layer with y<x; a Si layer of thickness h; a gate dielectric; and a highly conductive gate layer.

64. The method of claim 63, wherein h and y are approximately 0.

65. The method of claim 64, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y<x; a $Si_{1-w}Ge_w$ layer; a Si layer; a gate dielectric; and a highly conductive gate layer.

66. The method of claim 65, wherein y is approximately 0.

67. The method of claim 64, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y<x; a $Si_{1-w}Ge_w$ layer; a Si layer; and a highly conductive gate layer.

68. The method of claim 67, wherein y is approximately 0.

69. The method of claim 62, wherein the surface channel MOSFET comprises a $Si_{1-y}Ge_y$ layer with y>x, a $Si_{1-w}Ge_w$ layer; a Si layer; a gate dielectric; and a highly conductive gate layer.

70. The method of claim 69, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y>x; a $Si_{1-w}Ge_w$ layer; a Si layer; a gate dielectric; and a highly conductive gate layer.

71. The method of claim 70, wherein y is approximately 1.

72. The method of claim 69, wherein the buried channel FET comprises a $Si_{1-y}Ge_y$ layer with y>x; a $Si_{1-w}Ge_w$ layer; a surface Si layer; a highly conductive gate layer.

73. The method of claim 72, wherein y is approximately 1.

74. The method of claim 62, wherein the relaxed $Si_{1-x}Ge_x$ further comprises at least one planarized surface.

75. A method of fabricating a semiconductor circuit on a heterostructure, said heterostructure including a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a $Si_{1-y}Ge_y$ layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-w}Ge_w$ layer on said $Si_{1-y}Ge_y$ layer, and a Si layer on said $Si_{1-w}Ge_w$ layer, said method comprising:

integrating surface channel and buried channel devices on said heterostructure.

76. The method of claim 75, wherein a carrier channel of a surface channel device is provided in either said Si layer or said $Si_{1-y}Ge_y$ layer.

77. The method of claim 75, wherein the semiconductor structure is undoped.

78. The method of claim 75, wherein y<x.

79. The method of claims 76 or 78, wherein y is approximately 0.

80. The method of claim 75 further comprising planarizing at least one surface.

81. The method of claim 75, wherein the substrate comprises Si.

82. The method of claim 75, wherein the substrate comprises Si with a layer of SiO_2.

83. The method of claim 75, wherein the substrate comprises a graded composition SiGe layer on Si.

84. The method of claim 83, wherein the substrate further comprises a uniform composition $Si_{1-z}Ge_z$ layer on said graded composition layer.

85. The method of claim 84, wherein z is approximately equal to x.

86. The method of claim 85, wherein the surface of the substrate is planarized.

87. The method of claim 75, wherein the substrate comprises a uniform $Si_{1-z}Ge_z$ layer on Si.

88. The method of claim 87, wherein z is approximately equal to x.

89. The method of claim 88, wherein the surface of the substrate is planarized.

90. The method of claim 87, wherein the $Si_{1-z}Ge_z$ /Si structure is formed through wafer bonding.

91. The method of claim 87 further comprising a SiO_2 layer between the uniform $Si_{1-z}Ge_z$ layer and the Si.

92. The method of claim 91, wherein z is approximately equal to x.

93. The method of claim 92, wherein the surface of the substrate is planarized.

94. A method of fabricating a semiconductor circuit on a heterostructure, said heterostructure including a planarized relaxed $Si_{1-x}Ge_x$ layer on a substrate, and regrown device layers on said planarized relaxed $Si_{1-x}Ge_x$ layer, said method comprising:

integrating surface channel and buried channel devices on said heterostructure.

95. The method of claim 94, wherein the regrown device layers include a $Si_{1-y}Ge_y$ layer of thickness h; a $Si_{1-w}Ge_w$ layer; a $Si_{1-n}Ge_n$ layer having supply dopants; and a Si layer.

96. The method of claim 95, wherein h is approximately 0.

97. The method of claim 95, wherein w<x and the supply dopants are n-type.

98. The method of claim 94, wherein a carrier channel of a surface channel device is provided in either said Si layer or said $Si_{1-w}Ge_w$ layer.

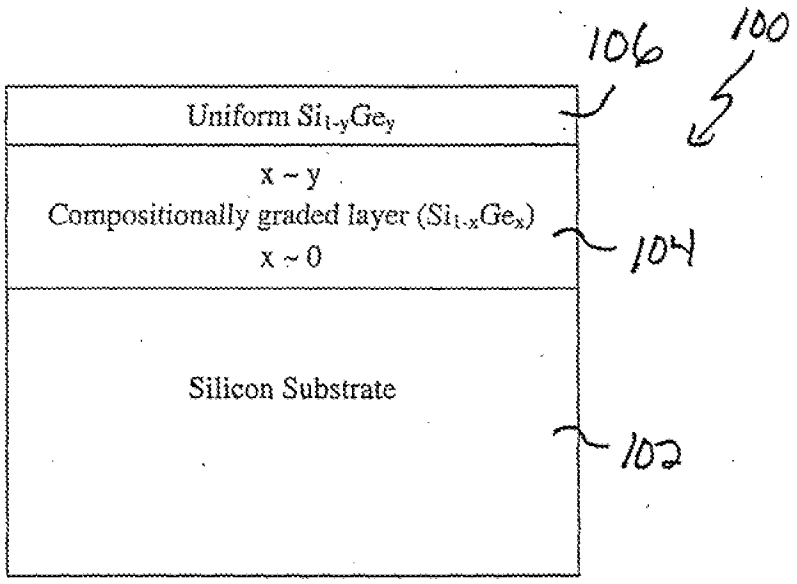

106
100
Uniform $Si_{1-y}Ge_y$
x ~ y
Compositionally graded layer ($Si_{1-x}Ge_x$)
x ~ 0
104
Silicon Substrate
102

FIG. 1

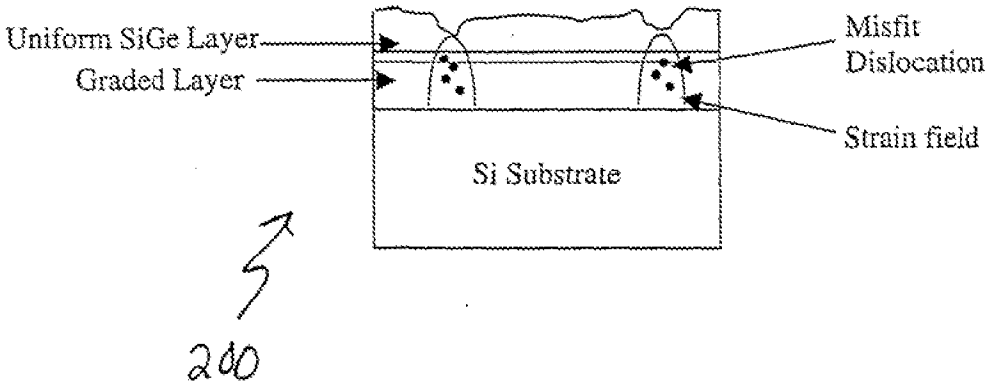
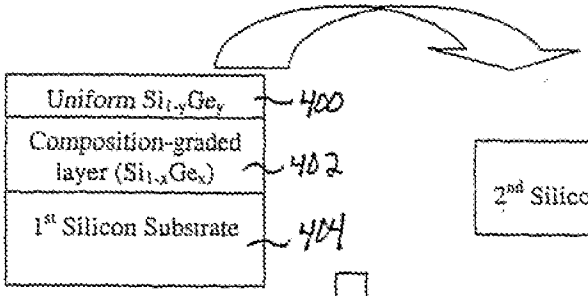

Uniform SiGe Layer
Graded Layer
Misfit
Dislocation
Strain field
Si Substrate
200

FIG. 2

Type of Surface	Average Roughness (nm)
As-grown graded composition relaxed SiGe	7.9
Planarized SiGe	0.57
Regrowth SiGe, lattice-matched	~0.6
Regrowth SiGe, slight mismatch, thickness =1.5μm	0.77

FIG. 3

FIG. 4A



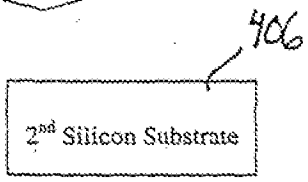


FIG. 4B

FIG. 4C

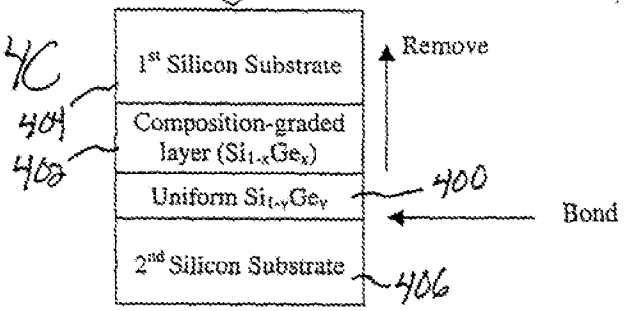


FIG. 4D

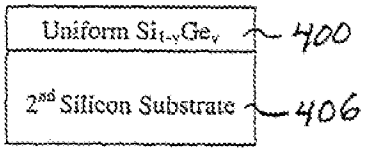


FIG. 5A

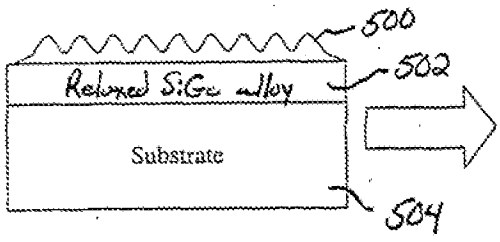


FIG. 5B

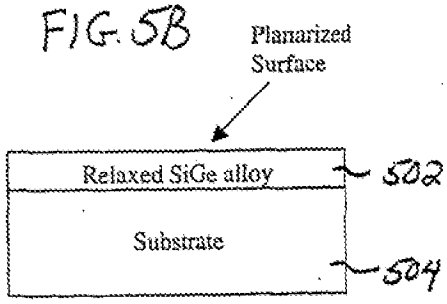


FIG. 5C

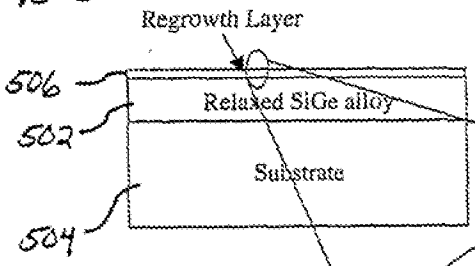


FIG. 5D

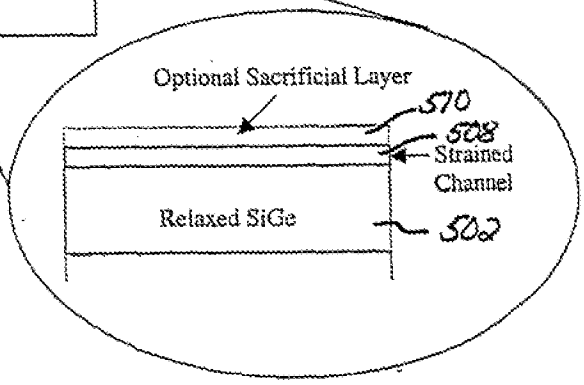


FIG.6A

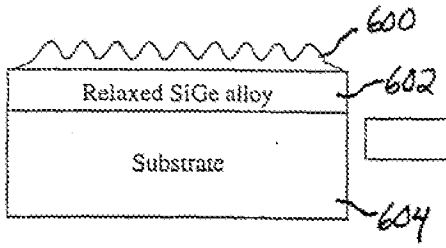


FIG.6B

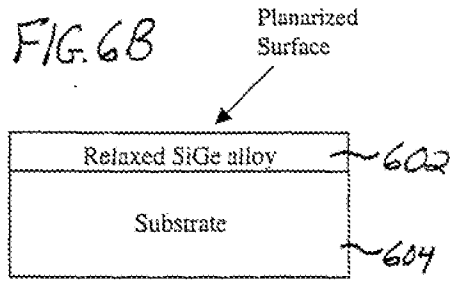


FIG.6C

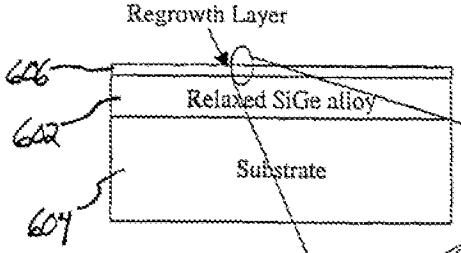


FIG.6D

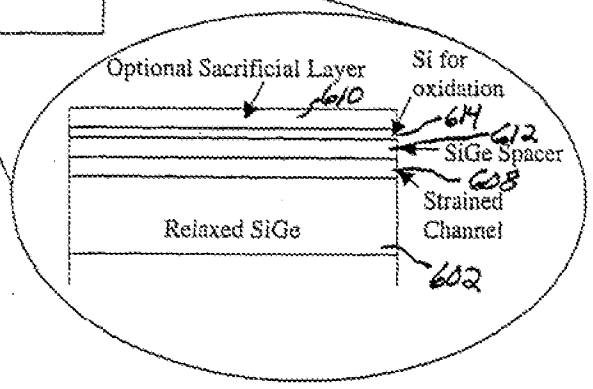


FIG. 7A

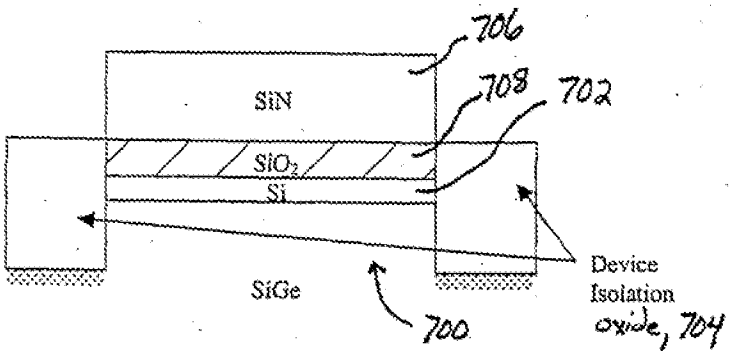

706
708
702
SiN
SiO_2
Si
SiGe
700
Device
Isolation
oxide, 704

FIG. 7B

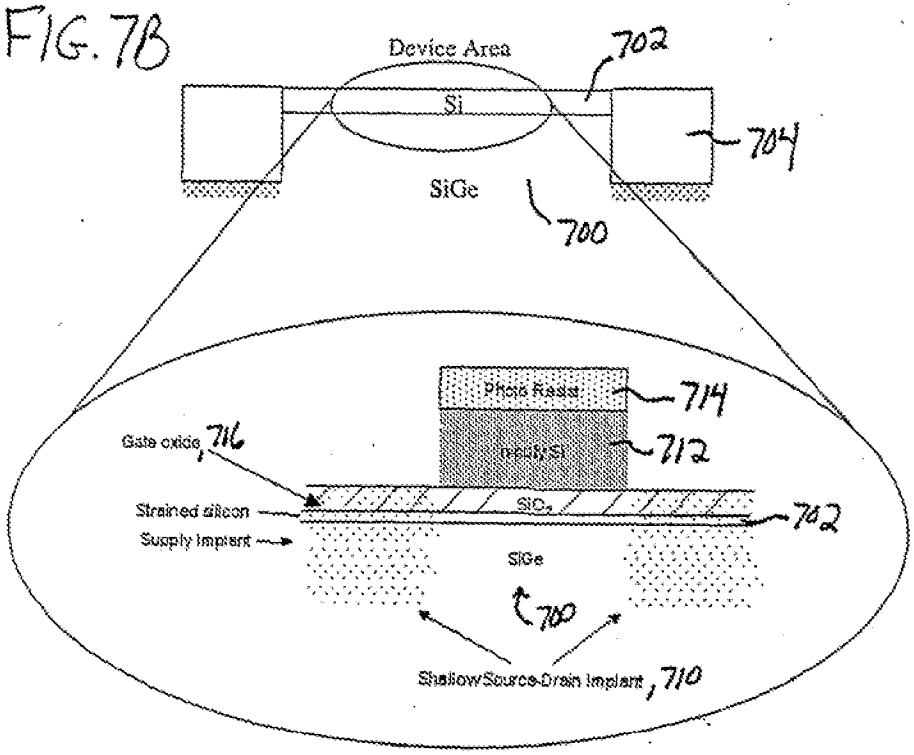

Device Area
702
Si
704
SiGe
700
Photo Resist
714
Gate oxide, 716
712
Strained silicon
Supply Implant
SiO_2
702
SiGe
700
Shallow Source-Drain Implant, 710

FIG. 7C

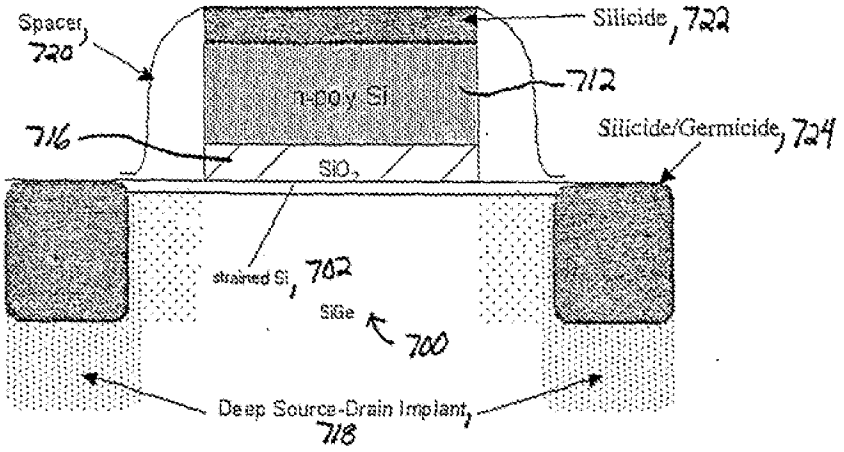

Spacer, 720
Silicide, 722
712
n-poly Si
716
Silicide/Germicide, 724
SiO2
strained Si, 702
SiGe
700
Deep Source-Drain Implant, 718

FIG. 7D

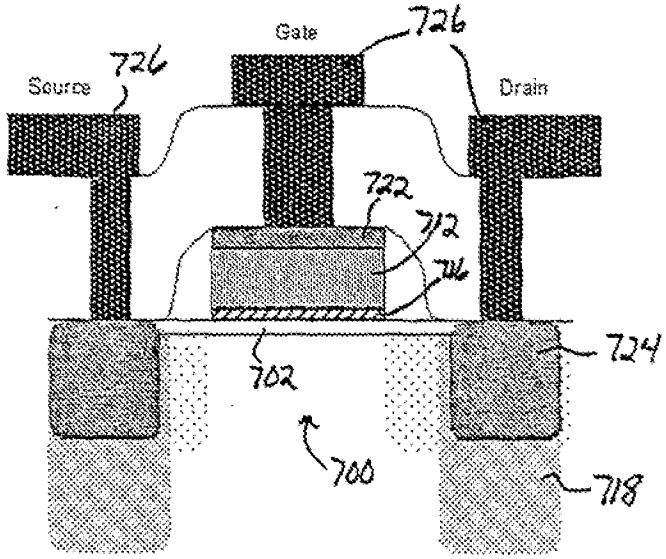

Gate
726
Source
726
Drain
722
712
716
724
702
700
718

FIG.8A

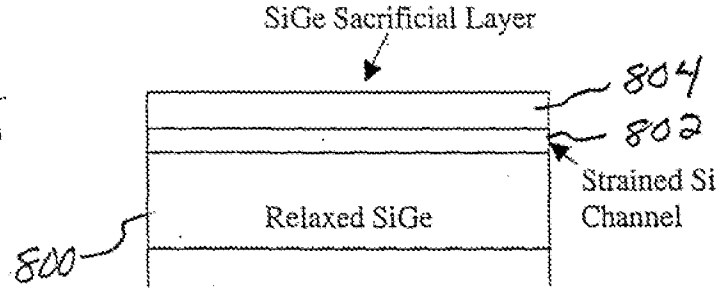

SiGe Sacrificial Layer
804
802
Strained Si
Channel
Relaxed SiGe
800

FIG.8B

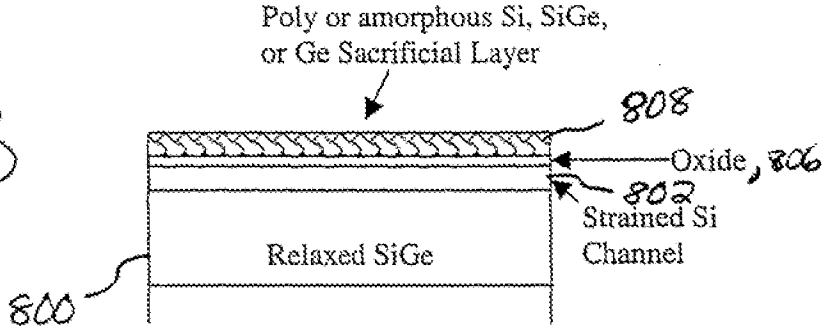

Poly or amorphous Si, SiGe,
or Ge Sacrificial Layer
808
Oxide, 806
802
Strained Si
Channel
Relaxed SiGe
800

FIG. 9A

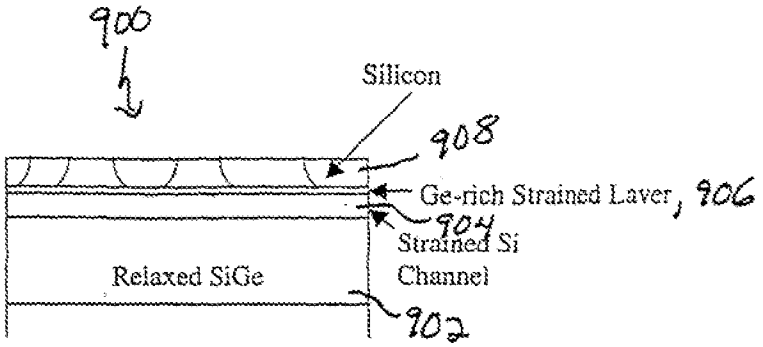
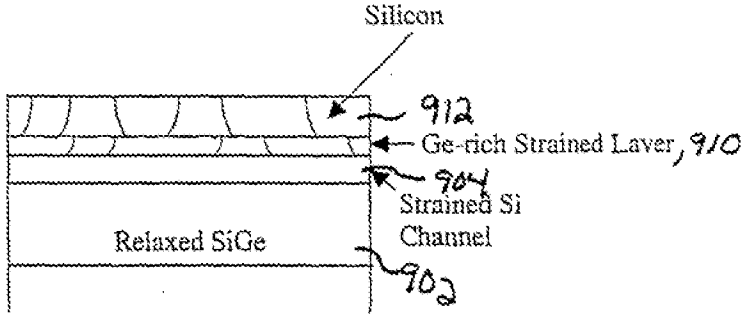

900
Silicon
908
Ge-rich Strained Laver, 906
904
Strained Si
Channel
Relaxed SiGe
902

FIG. 9B


Silicon
912
Ge-rich Strained Laver, 910
904
Strained Si
Channel
Relaxed SiGe
902

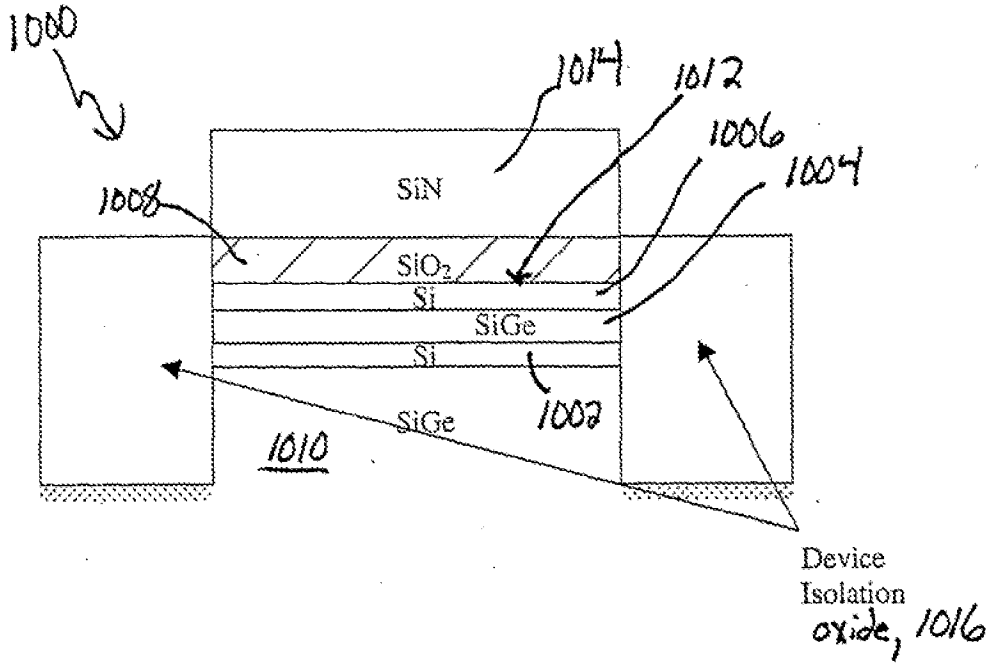

1000
1014
1012
1006
1004
1008
SiN
SiO2
Si
SiGe
Si
1002
SiGe
1010
Device
Isolation
oxide, 1016

FIG. 10

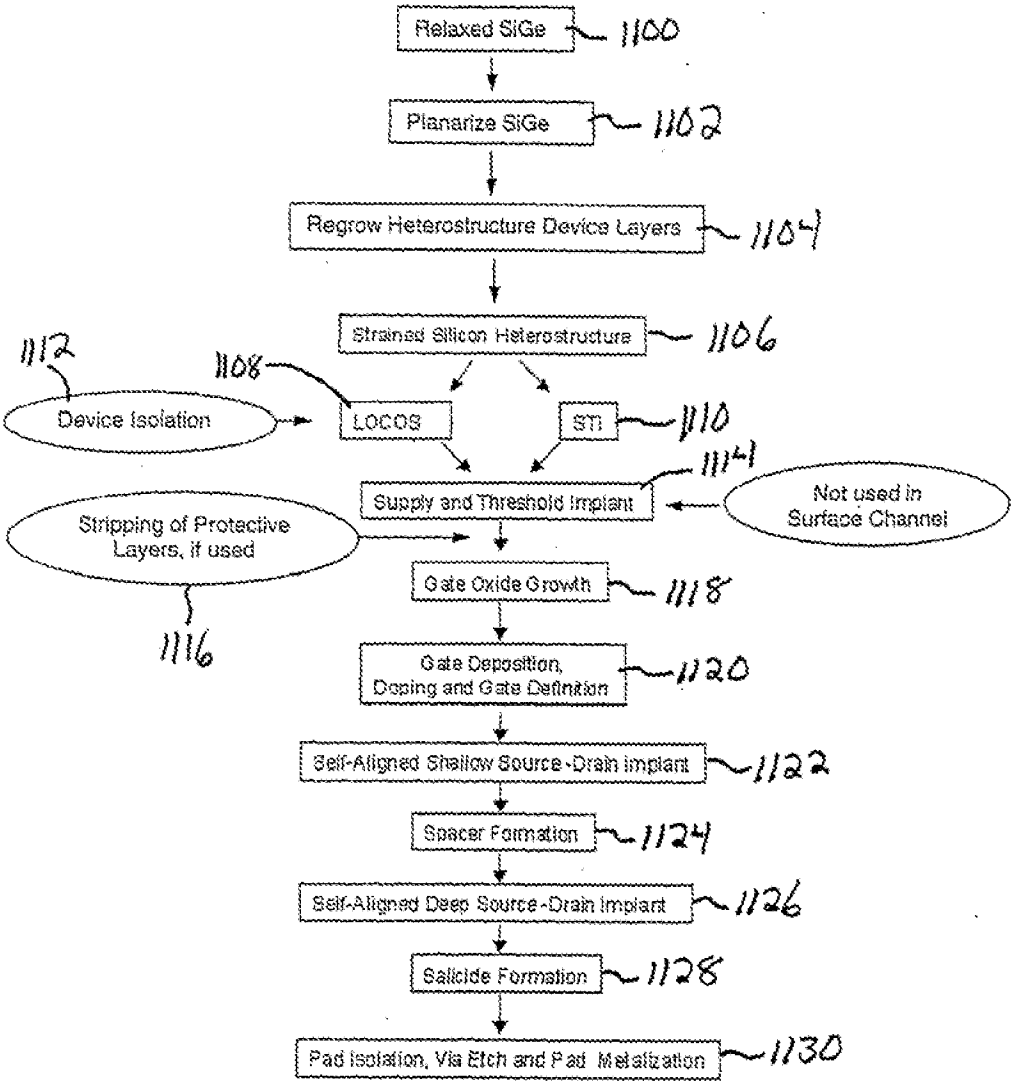

Relaxed SiGe
1100
Planarize SiGe
1102
Regrow Heterostructure Device Layers
1104
Strained Silicon Heterostructure
1106
1112
Device Isolation
1108
LOCOS
STI
1110
1114
Supply and Threshold Implant
Not used in Surface Channel
Stripping of Protective Layers, if used
1116
Gate Oxide Growth
1118
Gate Deposition, Doping and Gate Definition
1120
Self-Aligned Shallow Source-Drain Implant
1122
Spacer Formation
1124
Self-Aligned Deep Source-Drain Implant
1126
Salicide Formation
1128
Pad Isolation, Via Etch and Pad Metalization
1130

FIG. 11

FIG. 12A

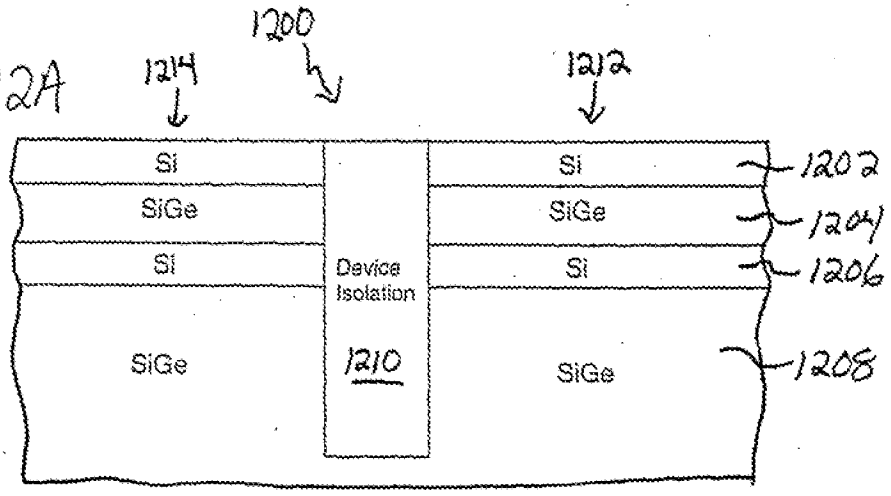


FIG. 12B

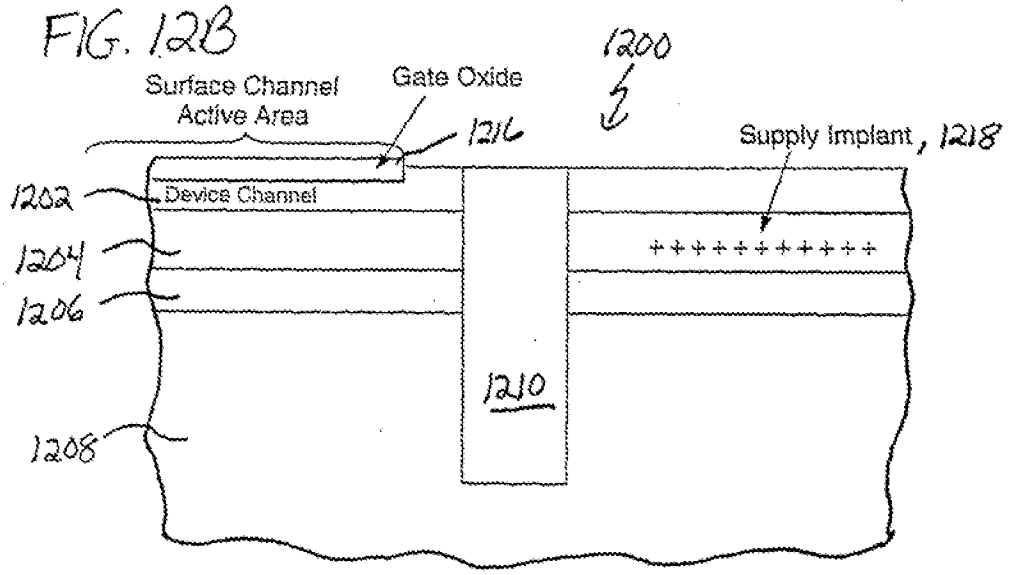


FIG. 12C

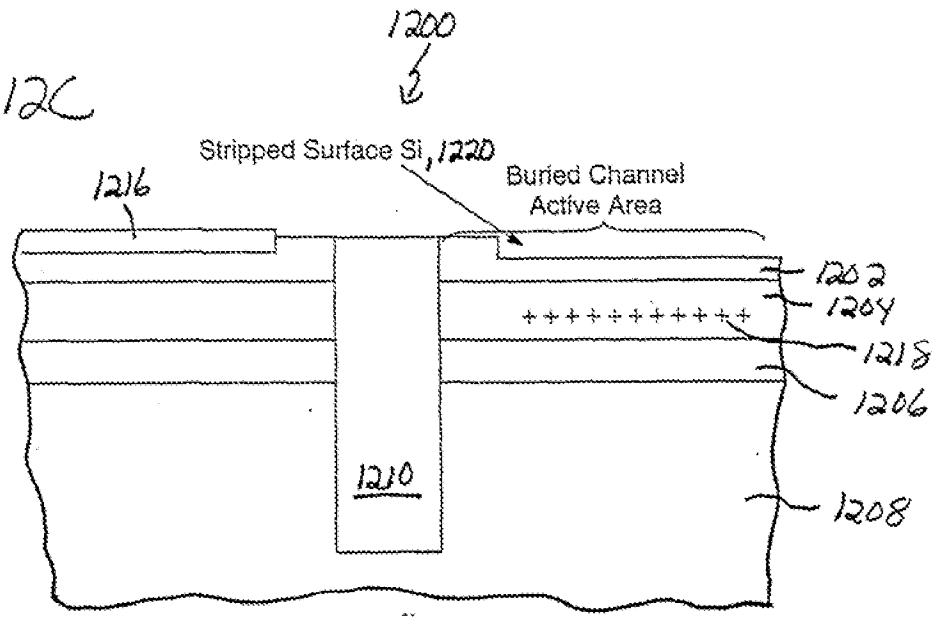


FIG. 12D

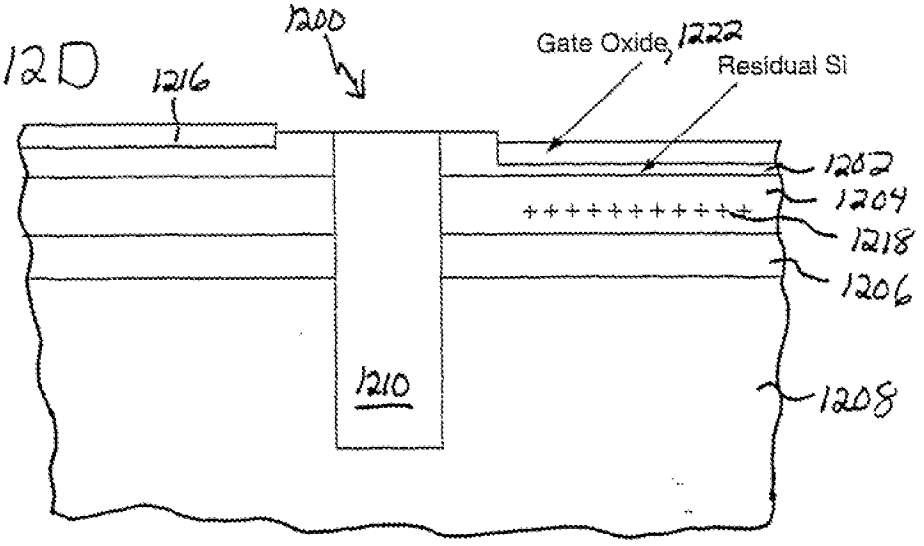


FIG. 13A

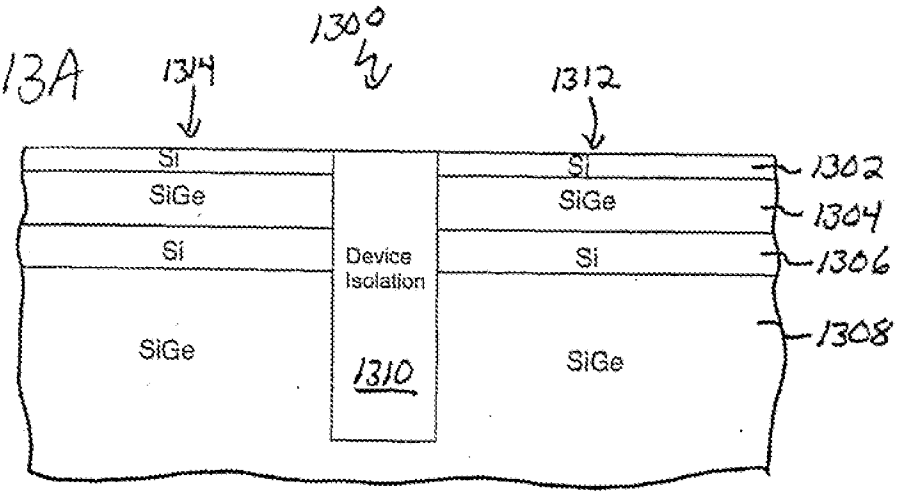


FIG. 13B

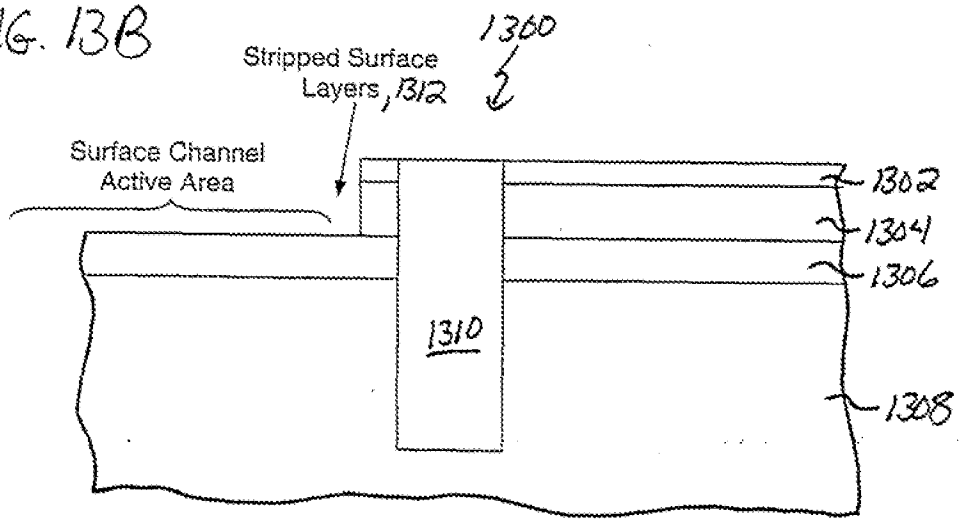


FIG. 13C

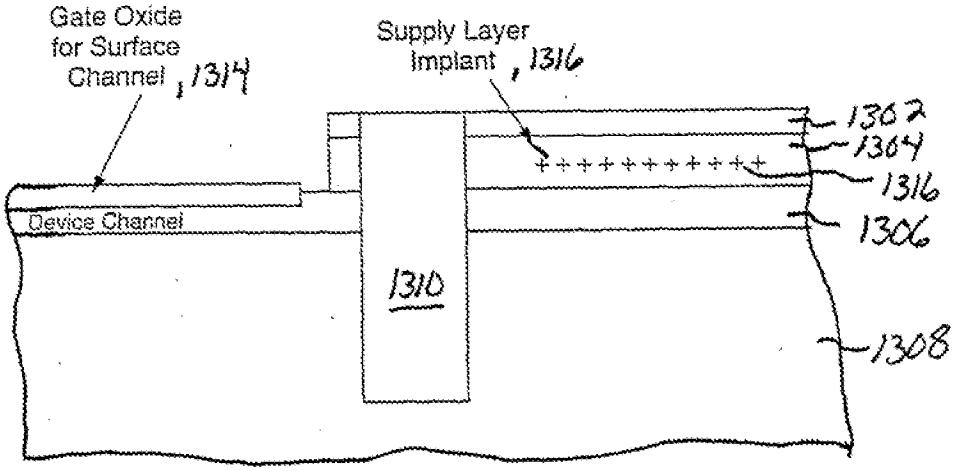


FIG. 13D

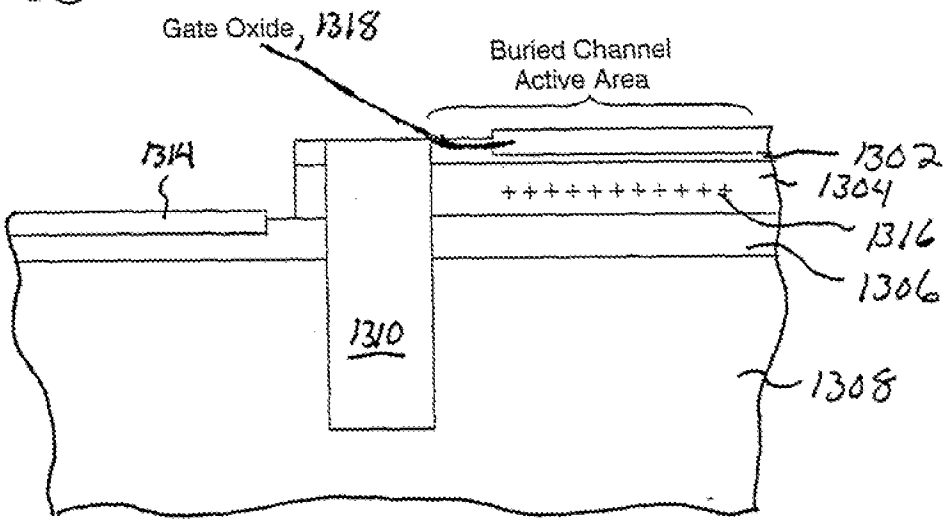


FIG. 14A

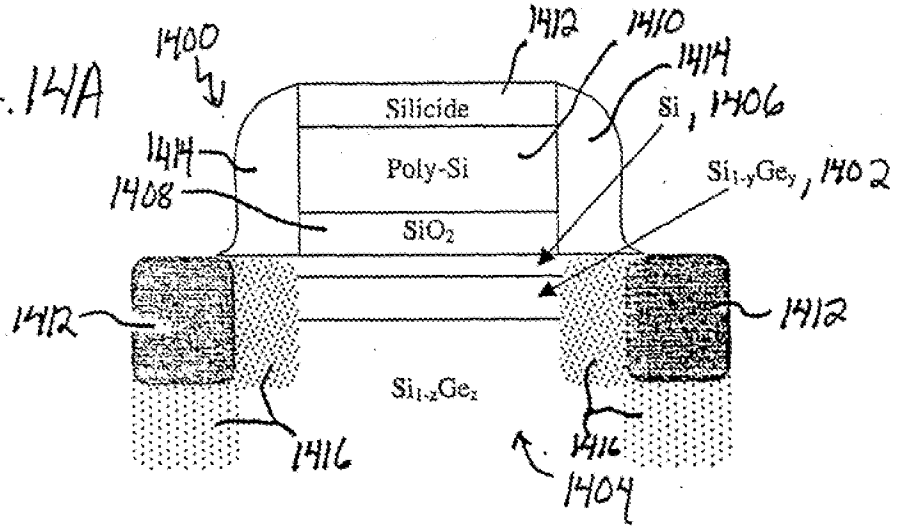
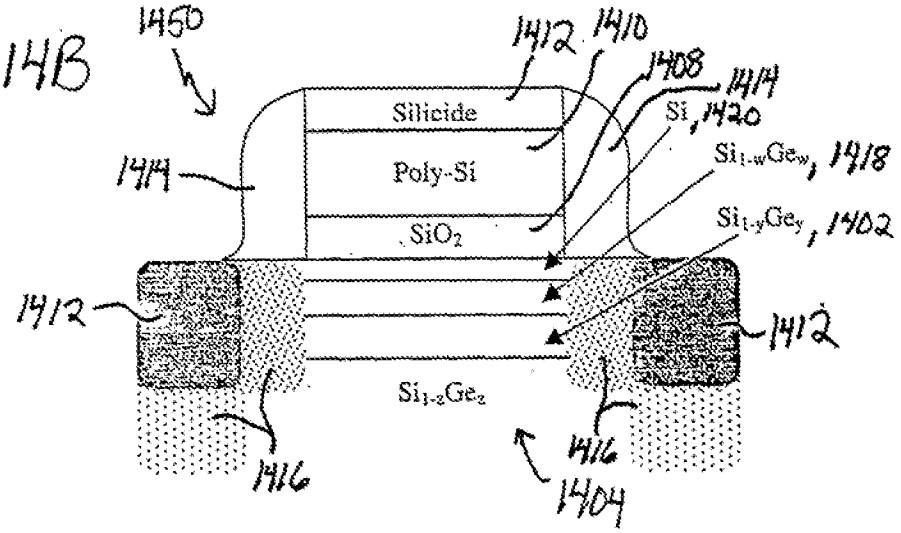


FIG. 14B



INTERNATIONAL SEARCH REPORT

Int ial Application No
PCT/US 02/03691

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/092 H01L29/778 H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, PAJ, INSPEC, EPO-Internal, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 683 522 A (IBM) 22 November 1995 (1995-11-22)	1-5, 7-11,13, 14,17, 18, 25-36, 38-42, 44-48, 50,51, 54,55, 62-73, 75-85, 87,88, 91-93
Y	column 5, line 19 -column 13, line 17; figures 1-8	6,12,15, 16, 19-24, 37,43, 49,52, 53,
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[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
3 July 2002	10/07/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Berthold, K

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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